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Research Assistant Professor
Midwest Institute of Nanoelectronics Discovery (MIND), University of Notre Dame

EDUCATION

1/04 ~ 7/07 ***National University of Singapore, Singapore***
- Ph.D. in Department of Electrical and Computer Engineering.
- Dissertation: Study of Advanced Gate Stack using High-K Dielectric and Metal Electrode.

3/01 ~ 2/03 ***Korea Aerospace University, Kyunggi-Do, Korea***
- M.S. in Materials Engineering.

3/94 ~ 2/01 ***Korea Aerospace University, Kyunggi-Do, Korea***
- B.S. in Materials Engineering.

9/95 ~ 2/98 ***Republic of Korea Air Force***
- Military Service, Honorable Discharged as an airman first class

RESEARCH EXPERIENCE

8/10 ~ Present ***Research Assistant Professor:*** *Midwest Institute of Nanoelectronics Discovery (MIND),* ***University of Notre Dame,*** *Notre Dame, IN*
- Investigating Graphene Nano-Ribbon (GNR) tunneling field effect transistor which is funded by Semiconductor Research Corporation's Nanoelectronics Research Initiative.
- Fabricated and characterized sub-10nm Graphene Nano-Ribbon in wafer size substrate, for the first time, showing a substantial bandgap and collaborating with Naval Research Laboratory (NRL) to improve the graphene transistors on SiC wafers.
- Developing a formation of graphene p-n junction by electrostatic, solid-electrolyte, and chemical bonding to the edges.
- Introducing ions (Li^+ & ClO^-_4) graphene device for logic and memory applications.
- Correlating the experimental results with device modeling and developing the model for the tunneling FET using experimental results.

8/07 ~ 7/10 ***Senior Engineer:*** *Process Development Team, Semiconductor R & D center,* ***Samsung Electronics****, Korea*
- Developed the NAND Flash Memory for the 40 to 20nm node in the area of tunneling oxide, inter poly dielectric, floating gate, and control gate for floating memory as well as charge trap flash (CTF).
- Improved the performance of SONOS and TANOS gate stack using plasma and high-K dielectrics. (Requiring knowledge of operation physics and holding one Korea patent).
- Set up the pilot device process of vertical memory for sub 10nm node as a main leadership (Requiring an understanding of lithography, CMP, dry and wet etch, annealing, implantation, CVD, PVD, ALD deposition, low-K materials, device physics and holding 4 Korea patents).
- Involved the project of high-K inter poly dielectric (IPD) for floating gate and high-k blocking oxide for charge trap flash (CTF).
- Analyzed the interface trap between inter poly dielectric (IPD) for the floating gate memory devices and suggested the *in-situ* deposition of IPD.
- Identified the effect of plasma nitridation on the surface of floating gate and developed the selective removal of un-wanted plasma nitridation residue. (One Korea patent and one U.S patent is filed).
- Set up Aixtron Atomic Layer Deposition (ALD) equipment and developed high-k dielectrics such as Al_2O_3, HfO_2, SiO_2, HfSiO, and AlSiO for memory and logic devices.
- Took responsibility for Atomic Layer Deposition (ALD) and Rapid Thermal Annealing (RTA) equipment.

1/04 ~ 7/07 ***Doctoral Research:*** *Department of Electrical and Computer Engineering,* ***National University of Singapore****, Singapore*

● Investigated formation of gate stack of metal electrode and high-K dielectrics.
● Examined various metal carbides such as HfC, TaC, WC, and VC for metal electrode and suggested HfC as a low work function electrode, resulting in presentation at VLSI 2007.
● Studied the hard mask effect during the metal electrode etching, leading to DPS 2005 Young Research Award.
● Examined the plasma etch residue effect on memory device using XPS and Certificated XPS super-user.
● Developed various high selectivity dry etching recipe for TaN, HfN,TiN, W, Ru, Pt, Ir, and poly-Si over HfO_2 gate dielectrics.
● Analyzed and developed the high selective etching of HfO_2 over Si substrate using low ion energy
● Took responsibility for plasma etcher, ashing, and PECVD equipment.

7/01 ~ 6/03 ***Assistant Researcher:*** *MEMS division,* ***Korea Electronics Technology Institute (KETI)****, Kyunggi-Do, Korea.*

● Investigated LIGA (lithography, electroplating, and molding) process for MEMS

HONORS

● **Dry Process Symposium (DPS) 2005 Young Research Award:** 27th International Symposium on Dry Process, sponsored by The Institute of Electrical Engineers of Japan and The Japan Society of Applied Physics, November 2006 in Nagoya, Japan

● **Dorothy M. and Earl S. Hoffman Travel Grants:** American Vacuum Society (AVS) 52nd International Symposium, Boston, USA, 2005

TECHNICAL EXPERIENCE

- Analyzed and characterized the device performance of memory and logic device with advanced device physics.
- Broad knowledge and experiences not only gate dielectrics, metal electrode, and plasma etching but also CMP, and lithography, and low-k materials to fabricate the device of the leading company level
- Fabrication of Graphene Nano-Ribbon (GNR) field effect transistor experience using various equipment
- Electron beam lithography experience for 10nm width patterns process
- Plasma etching and plasma related equipment experience with optical emission tools
- Atomic layer deposition (ALD) and rapid thermal annealing (RTA) experience to improve the device performance of next generation memory.
- Proficient in using various measurement tools such as HP and Keithley series

PUBLICATIONS, PATENTS, & PRESENTATIONS

Refereed articles

● G. Zhou, Y. Lu, R. Li, W. S. Hwang, Q. Liu, Q. Zhang, T. Vasen, C Chen, H. Zhu, J. Kuo, S. Koswatta, T. Kosel, M. Wistey, A. Seabaugh and H Zing. "Vertical InGaAs/InP tunnel FETs with tunneling normal to the gate" *Electron Device Letters* EDL 32 (2011)

● W. S. Hwang, D. S. H. Chan, and B. J. Cho, "Metal Carbides for Band-Edge Work Function Metal Gate CMOS Devices", *Transactions on Electron Devices 55, 2469 (2008.)*

● W. S. Hwang, B. J. Cho, D. S. H. Chan, S. W. Lee, and W. J. Yoo, "Effects of Volatility of Etch By-products on Surface Roughness During Etching of Metal Gates in Cl_2", *J. Electrochemical Society 155, H6 (2008)*

● G. Zhang, W. S. Hwang, S. -H. Lee, B. –J. Cho, and W. J. Yoo, "Endurance Reliability of Multilevel-Cell Flash Memory Using a ZrO_2/Si_3N_4 Dual Charge Storage Layer", *Transactions on Electron Devices 55, 2361 (2008).*

● Y. Q. Wang, W. S. Hwang, G. Zhang, G. Samudra, Y. –C. Yeo, and W. J. Yoo, "Electrical Characteristics of Memory Devices with High-k HfO_2 Trapping Layer and Dual Tunneling Layer SiO_2/Si_3N_4". *Transactions on Electron Devices 54, 2699 (2007).*

● A. E.-J. Lim, R. T. P. Lee, X. P. Wang, W. S. Hwang, C. H. Tung, G. S. Samudra, D.-L. Kwong, and Y.-C. Yeo, "Yttrium- and Terbium-based Interlayer on SiO_2 and HfO_2 Gate Dielectrics for Work Function Modulation of Nickel Fully-Silicided Gate in NMOSFETs", *Electron Device Letters 28, 482 (2007)*

● W. S. Hwang, B.-J. Cho, D. S. H. Chan, and W. J. Yoo, "Low Energy N_2 Ion Bombardment for the Removal of $(HfO_2)_x(SiON)_{1-x}$ in Dilute HF, *J. Vac. Sci. Technol A 25, 1056 (2007)*.

● Andy E. –J. Lim, W. S. Hwang, X. P. Wang, Doreen M. Y. Lai, G. S. Samudra, D. –L. Kwong, and Y. –C. Yeo, "Metal Gate Work Function Modulation Using Hafnium Alloys obtained by the Interdiffusion of Thin Metallic Layers", *J. of the Electrochemical Society 154, (2007).*

● W. S. Hwang, B. –J. Cho, D. S. H. Chan, Vladimir Bliznetsov, and W. J. Yoo, "Effects of SiO_2/Si_3N_4 Hard Masks on Etching Properties of Metal Gates", *J. Vac. Sci. Technol B 24, 2689 (2006).*

● W. S. Hwang, H. H. Ngu, W. J. Yoo and V. Bliznetsov, "Chemical analysis of etching residues in metal gate stack for CMOS process", *Studies in Surface Science and Catalysis 159 (new developments and application in chemical reaction engineering) 365, Elsevier, Netherlands (2006).*

● W. S. Hwang, J. H. Chen, W. J. Yoo, and V. Bliznetsov, "Investigation of Etching Properties of Metal-nitride/High-K Gate Stacks Using Inductively Coupled Plasma", *J. Vac. Sci. Technol A 23, 964 (2005).*

Patents

● J. W. Choi, W. S. Hwang, G. H. Choi, E. Hong, J. S. Goo, and B. Y. Lee (Samsung Electronics Co, Ltd.), "Methods of Manufacturing Flash Memory Devices by Selective Removal of Nitrogen Atoms", US20110256708, *USA*.

● W. S. Hwang, T. Nakanisi, D. C. Yoo, G. H. Hwang, H. M. Choi, C. J. Park, (Samsung Electronics Co, Ltd.), "Three-Dimensional Semiconductor Device", *Korea patent 10-2011-0108216.*

● J. W. Choi, W. S. Hwang, G. H. Choi, E. G. Hong, J. S. Goo, B. Y. Lee (Samsung Electronics Co, Ltd.), "Flash Memory Device Manufacturing Method", *Korea patent 10-2011-0114970.*

● C. J. Park, G. H, Hwang, H. M. Choi, D. C. Yoo, and W. S. Hwang, (Samsung Electronics Co, Ltd.), "Three-Dimensional Semiconductor Device and Manufacturing Method", *Korea patent 10-2011-0108220.*

● C. J. Park, D. C. Yoo, T. Nakanisi, G. H, Hwang, H. M. Choi, and W. S. Hwang, (Samsung Electronics Co, Ltd.), "Three-Dimensional Semiconductor Device and Manufacturing Method", *Korea patent 10-2011-0108219*.

● S. J. Kim, J. C. Lee, B. Y. Goo, W. S. Hwang, J. G. Lee, and J. H. Kim (Samsung Electronics Co, Ltd.), " Semiconductor device and associated methods of manufacture", *Korea patent 10-2010-0101450.*

● J. S. Park, W. S. Hwang, S. S. Park, J. W. Cho, S. W. Chung and I. G. Lee (Korea Electronics Technology Institute), "Micro Mold and Manufacturing Method for Micro Part Replication", *Korea Patent 10-2003-0028246.*

Presentations

● A. Seabaugh, S. D. Chae, P. Fay, W. S. Hwang, T. Kosel, R. Li, Q. Liu, Y. Lu, T. Vasen, M. Wistey, H. Xing, G. Zhou, and Q. Zhang (invited), "III-V Tunnel Field-Effect Transistors", ESC, Boston (Sep. 26-29, 2011)

● A. Seabaugh, S. D. Chae, P. Fay, W. S. Hwang, T. Kosel, R. Li, Q. Liu, Y. Lu, T. Vasen, M. Wistey, H. Xing, G. Zhou, Q. Zhang, and R. M. Wallace (invited), "Interface Traps and Low Subthreshold Swing in III-V Tunnel FETs", AVS 58th International Symposium, Nashville, Tennessee (Oct30-Nov4, 2011)

● K. Tahy, W. S. Hwang, J. L. Tedesco, R. L. Myers-Ward, P. M. Campbell, C. R. Eddy Jr., D. K. Gaskill, H. Xing, A. C. Seabaugh, and D. Jena, "Large Scale Fabrication of Sub-10 nm Graphene Nanoribbon Field Effect Transistors", Techcon 2011, Austin, Texas (Sep 12-13, 2011).

● K. Tahy, W. S. Hwang, J. L. Tedesco, R. L. Myers-Ward, P. M. Campbell, C. R. Eddy Jr., D. K. Gaskill, H. Xing, A. C. Seabaugh, and D. Jena, "Sub-10nm Epitaxial Graphene Nanoribbon FETs",
2011 Device Research Conference, Santa Barbara, CA (June 20-22, 2011)

● G. Zhou, Y. Lu, R. Li, Q. Zhang, W. S. Hwang, Q. Liu, T. Vasen, H. Zhu, J. Kuo, S. Koswatta, T. Kosel, M. Wistey, P. Fay, A. Seabaugh, and H. Xing, "Self-aligned InAs/Al0.45Ga0.55Sb vertical tunnel FETs", 2011 Device Research Conference, Santa Barbara, CA (June 20-22, 2011)

● G. Zhou, Y. Lu, R. Li, T. Vasen, Q. Liu, W. S. Hwang, Q. Zhang, H. Zhu, J. –M. Kuo, S. Koswatta, M. Wistey, T. Kosel, P. Fay, A. Seabaugh, and H. Xing, "Passivation Effects of ALD Oxides on Self-Aligned In0.53Ga0.47As/InAs/InP Vertical Tunnel FETs", 2011 Electronic Materials Conference, Santa Barbara, CA (June 22-24, 2011)

● W. S. Hwang, K. Tahy, J. L. Tedesco, R. L. Myers-Ward, P. M. Campbell, C. R. Eddy Jr., D. K. Gaskill, H. Xing, A. C. Seabaugh, and D. Jena, "Fabrication of Top-Gated Sub-10 nm Epitaxial Graphene Nanoribbon FETs Using Hydrogen Silsesquioxane(HSQ)", 2011 Electronic Materials Conference, Santa Barbara, CA (June 22-24, 2011)

● G. Zhou, Y. Lu, R. Li, W. Hwang, Q. Zhang, Q. Liu, T. Vasen, C. Chen, H. Zhu, J. Kuo, S. Koswatta, T. Kosel, M, Wistey, P. Fay, A. Seabaugh, and H. Xing, "Self-aligned In0.53Ga0.47As/InAs/InP vertical tunnel FETs", Int. Conf. Compound Semicond. Manuf. Technol., CA, USA (May 16~19, 2011)

● K. Tahy, W. S. Hwang, J. L. Tedesco, R. L. Myers-Ward, P. M. Campbell, C. R. Eddy Jr., D. K. Gaskill, H. Xing, A. C. Seabaugh, and D. Jena, " Control of the Unintentional Doping in Epitaxial Graphene FETs" Graphene 2011, Bilbao, Spain (Apr 11-14, 2011)

● D. H. Lee, S. D. Chae, W. S. Hwang, C. H. Shin, and W. S. Han, "Study on the treatment of Al_2O_3/SiO_2 CTF Blocking Oxide using Neutral Beam.", *The 31st Samsung Semiconductor Technology Symposium (2008)*

● G. Zhang, W. S. Hwang, S. M. Bobade, S. –H. Lee, B. –J. Cho, and W. J. Yoo, "Novel ZrO2/Si3N4 Dual Charge Storage Layer to Form Step-Up Potential Wells for Highly Reliable Multi-Level Cell Application" ,*International Electron Devices Meeting (IEDM) 2007, December 2007 in Washington, DC, USA.*

● X. P. Wang, M. –F. Li, H. Y. Yu, J. J. Yang, C. X. Zhu, W. S. Hwang, W. Y. Loh, A. Y. Du, J. D. Chen, A. Chin, S. Biesemans, G. Q. Lo, and D. –L. Kwong, "Highly Manufacturable CMOSFETs with Single High-k (HfLaO) and Dual Metal Gate Integration Process" *2007 International Conference on Solid State Devices and Materials (SSMD), September 2007 in Ibaraki, Japan.*

● B. J. Cho, W. S. Hwang, and D. S. H. Chan (Invited) "Metal Carbide Electrodes for Gate-First Metal Gate CMOS Process" *4th International Symposium on Advanced Gate Stack Technology, September 2007 in Austin, Texas, USA.*

● A. E.-J. Lim, R T. P. Lee, X. P. Wang, W. S. Hwang, C.-H. Tung, D. M. Y. Lai, G. Samudra, D.-L. Kwong, and Y.-C. Yeo "Band Edge NMOS Work Function for Nickel Fully-Silicided (FUSI) Gate Obtained by the Insertion of Novel Y-, Tb-, and Yb-based Interlayers" *37th European Solid-State Device Research Conference (ESSDERC), September 2007 in Munich, Germany.*

● W. S. Hwang, C. Shen, X. P. Wang, Daniel S. H. Chan, and B. J. Cho, "A novel hafnium carbides (HfCx) metal gate electrode for NMOS device application", *2007 Symposium on VLSI Technology, June 2007 in Kyoto, Japan.*

● Y. Q. Wang, D. Y. Gao, W. S. Hwang, C. Shen, G. Zhang, G. Samudra Y. –C. Yeo, and W. J. Yoo
"Fast erasing and highly reliable MONOS type memory with HfO_2 high-k trapping layer and Si_3N_4/SiO_2 tunneling stack" *International Electron Devices Meeting 2006, December 2006 in San Francisco, USA.*

● V. N. Bliznetsov, L. K. Bera, W. S. Hwang, N. Balasubramaniam, R. Kumar, G.-Q. Lo, A. D. Trigg, L.Y.Wong, K.M. Hoe "Triple Hard Mask Approach for Etching of Sub-30 nm Metal Gates", *28th International Symposium on Dry process, November 2006 in Nagoya, Japan.*

● W. S. Hwang, B. –J. Cho, D. S. H. Chan and W. J. Yoo "Study on Nonvolatile Byproducts Generated during Etching of Advanced Gate Stacks" *28th International Symposium on Dry process, November 2006 in Nagoya, Japan.*

● W. S. Hwang, V. N. Bliznetsov, B. –J. Cho, D. S. H. Chan and W. J. Yoo "Damage Free Etching of RuO_2 in O_2/He plasma" *28th International Symposium on Dry process, November 2006 in Nagoya, Japan.*

● W. S. Hwang, W. J. Yoo, B. J. Cho, and D. S. H. Chan "Effects of Low Energy Nitrogen Plasma on the Removal of HfSiON" *AVS 53rd International Symposium, November 2006 in San Francisco, CA, USA.*

● Andy E. –J. Lim, W. S. Hwang, X. P. Wang, D. –L. Kwong, and Y. –C. Yeo "Work Function Modulation Using Thin Interdiffused Metal Layers for Dual Metal-Gate Technology" *2006 International Conference on Solid State Devices and Materials (SSMD), September 2006 in Yokohama, Japan.*

● Fei Gao, S. Balakumar, Li Rui, S. J. Lee, C. –H. Tung, T. Sudhiranjan, W. S. Hwang, N. Balasubramanian, D. –L. Kwong, and D. –Z. Chi "Pt-Germanosilicide Schottky S/D PMOSFET on SGOI Substrate Fabricated by Novel Condensation Approach" *13rd International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), July 2006, Singapore.*

● X. P. Wang, C. Shen, M.-F. Li, H. Y. Yu, Y. Sun, Y. P. Feng, Andy Lim, W. S. Hwang, Albert Chin,Y. C. Yeo, Patrick Lo , D.L.Kwong "Dual Metal Gates with Band-Edge Work Functions on Novel HfLaO High- κ Gate Dielectric" *2006 Symposium on VLSI Technology, June 2006 in Hawaii, USA.*

● Y. Q. Wang, P. K. Singh. W. J. Yoo, Y. C. Yeo, G. Samudra, Albert Chin, W. S. Hwang, J. H. Chen, S. J. Wang, D. –L. Kwong "Long Retention and Low Voltage Operation Using IrO_2/HfAlO/HfSiO/HfAlO Gate Stack for Memory Application", *International Electron Devices Meeting 2005, December 2005 in Washington, D. C., USA.*

● H. H. Ngu, W. S. Hwang, and W. J. Yoo, "Etching properties of High Work Function of IrO_2 in Cl2/SF6 plasma for CMOS Application", *27th International Symposium on Dry Process, November 2005 in Jeju, Korea.*

● W. S. Hwang, H. H. Ngu, G. Zhang, V. N. Bliznetsov, and W. J. Yoo, "Effect of SiO_2 Mask on Surface Properties of Advanced Gate Stacks Using ICP of Cl_2 / HBr", *27th International Symposium on Dry Process, November 2005 in Jeju, Korea,* (DPS 2006 Young Research Award)

● W. S. Hwang, Y. Q. Wang, W. J. Yoo, and V. Bliznetsov, "ICP Etching of p-type Conducting Materials with High Work Function for CMOS Application", *AVS 52nd International Symposium, October 2005 in Boston, MA, USA.*

● W. S. Hwang and W. J. Yoo "Effects of Non-Volatility of Etch Products on Surface Roughness during Etching of Advanced Gate Stack Materials" *AVS 52nd International Symposium, October 2005 in Boston, MA, USA.*

● W. S. Hwang, J. H. Chen, W. J. Yoo, and Z. L. Yuan "The surface roughening and residues formation during the etching of metal nitrides using Cl_2/HBr/O_2 inductively coupled plasma", *3rd International Conference on Materials for Advanced Technologies, July 2005 in Singapore.*

● J. H. Chen, W. S. Hwang, W. J. Yoo, and D. SH. Chan "Etch residues generated from Cl_2 / HBr inductively coupled plasma etching of Hf based high-k dielectrics", *3rd International Conference on Materials for Advanced Technologies, July 2005 in Singapore.*

● B. J. Cho, C. S. Park, P. W. Lwin, S. Y. Wong, J. Pu, W. S. Hwang, L. J. Tang, W. Y. Loh, and D. –L. Kwong "Dual Metal Gate Process Scheme for Wide Range Work Function Modulation and Reduced Fermi Level Pinning" *3rd International Conference on Materials for Advanced Technologies, July 2005 in Singapore.*

● C. S. Park, B. J. Cho, W. S. Hwang, W. Y. Loh, L. J. Tang, and D. –L. Kwong, "Dual Metal Gate Process by Metal Substitution of Dopant-Free Polysilicon on High-K Dielectric", *2005 Symposium on VLSI Technology, June 2005 in Kyoto, Japan.*

● W. S. Hwang, J. H. Chen, W. J. Yoo, and V. Bliznetsov, "Chemical analysis of etching residues in metal/high-k gate stacks CMOS process", *The 4th Asia-Pacific Chemical Reaction Engineering Symposium, June 2005 in Gyeongju, Korea.*

● W. S. Hwang, J. H. Chen, W. J. Yoo, D. S. H. Chan, and D. –L. Kwong, "Development of Post Etching Process for Hf Based High-K Gate Dielectric", *AVS 51st International Symposium, November 2004 in Anahelm, CA, USA.*

● J. H. Chen, W. S. Hwang, W. J. Yoo, D. S. H. Chan, and D. –L. Kwong, "Study of Refractory Metal Nitrides / HfO_2 Gate Stack Etching Using Inductively Coupled Plasma", *AVS 51st International Symposium, November 2004 in Anahelm, CA, USA.*

● J. H. Chen, W. S. Hwang, W. J. Yoo, and D. S. H. Chan, "Investigation of Etching Properties of HfSiO and HfSiON as Gate Dielectrics", *AVS 51st International Symposium, November 2004 in Anahelm, CA, USA.*