Suman Datta

Chang Family Chair Professor of Engineering Innovation
Department of Electrical Engineering
University of Notre Dame
271 Fitzpatrick Hall, Notre Dame, IN 46556
Phone: 574-631-8835 (fax: 574-631-4393)
E-mail: sdatta@nd.edu; Lab website: http://www.ndcl.ee.psu.edu/

Education

PhD, Electrical and Computer Engineering Dept., University of Cincinnati, OH, September 1999

Bachelors, Electrical Engineering Dept., Indian Institute of Technology, Kanpur, India, June 1995

Experience

Chair Professor (2015 – Present)

Department of Electrical Engineering, University of Notre Dame, IN

Professor (2011 – 2015)

Department of Electrical Engineering, Penn State University, PA

Monkowski Associate Professor (Career Development Professorship) (2007-2011)

Department of Electrical Engineering, Penn State University, PA

Principal Engineer (2005-2007)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Senior Staff Engineer (2003-2005)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Staff Engineer (2002-2003)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Senior Process Engineer (1999-2002)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Technology CAD (TCAD) Engineer (1999)

Avanti Corporation (now Synopsis), Fremont, CA

Technology Consultant for TSMC (Taiwan Semiconductor Manufacturing Corp), UMC (United Microelectronics Corp) and Samsung Electronics (2008 – Present)

Research Grants

Funding to date (Candidate's share = $8,102,354):

– 1 NRI grant **(**The Midwest Institute for Nanoelectronics Discovery: Energy Efficient Transistor and Architecture Center (2007-2012)

– 8 NSF grants (including premier Research Centers like i) Nanosystem Engineering Research Center (NERC) for Advanced Self Powered Systems of Integrated Sensors and Technologies; ii)

Expedition in Computing for Visual Cortex on Silicon; iii) Center for Nanoscale Science – MRSEC center; iv) Emerging Frontiers in Research and Innovation 2014 (EFRI-2014) on Two-Dimensional Atomic-layer Research and Engineering (2-DARE))

– 3 DARPA/SRC grants (Center for Low Energy Systems, LEAST FCRP, at Notre Dame; Materials, Structures and Devices (MARCO MSD Center) at MIT)

– 2 ONR, 2 DTRA, 1 NIST and 2 NSA grants

– 13 Industry grants (including Fortune 500 companies like Intel, Samsung, TSMC, Lam Research, Applied Materials, Global Foundries, Qualcomm)

Total number of publications to date:

– 212 total (100 journal, 112 refereed conferences)

– h-index = 45 with 7,113 citations (Google Scholar)

Total number of graduate students to date:

Postdoctoral: **5 completed**, **1 current**

PhD: **17 graduated**, **6 current** (including 2 IBM PhD Fellows, 1 Lam research PhD Fellow);

MS**: 7 graduated** (with thesis option), 0 current

Total number of issued United States patents: **165**

Current Research Interests

- Extending CMOS (e.g. germanium, compound semiconductor channel FinFETs)
- Beyond CMOS (e.g. tunneling transistors, ferroelectric transistors)
- Millimeter Wave Electronics (e.g. graphene ambipolar mixers and amplifiers)
- Correlated Oxide Electronics (e.g. coupled oscillators, phase transition FETs and RF switches)
- Co-Design of Emerging Devices, Circuits and Architecture (e.g. heterogeneous core processor)
- Neuromorphic or Cognitive Processors (e.g. visual cortex on a chip)
- Energy constrained Computing for Internet-of-Things (IOT) (e.g. non-volatile processors)

Awards and Honors

- Penn State Engineering Alumni Society (PSEAS) Premier Research Award (2015)
- IEEE Fellow for “contributions to for contributions to high-performance advanced silicon and compound semiconductor transistor technologies” (2013)
- SEMI Award for North America “in recognition of their pioneering work in the development, integration and introduction of a successful high-k dielectric and metal electrode gate stack for 45 nm CMOS IC production” (2012)
- IBM Faculty Award (2012)

- Penn State Engineering Alumni Society (PSEAS) Outstanding Research Award (2012)
- Distinguished Lecturer of IEEE Electron Devices Society (2011)
- Joseph Monkowsky Professorship for Faculty Early Career Development, The Pennsylvania State University (2007)
- Intel Achievement Award (the highest technical honor at Intel) for "developing the world's first high-K/metal gate CMOS transistors with record-setting performance" (2003)
- Divisional Achievement Award from Intel Logic Technology Development Group for "invention and successful demonstration of high performance Tri-gate CMOS transistors" (2002)
- All India Rank of 124 (Eastern Zone Rank: 18) among 300,000 students who appeared for Indian Institute of Technology Joint Entrance Examination (IIT-JEE) (1995)

Funded Projects

NRI

- Energy Efficient Transistor and Architectures, (06/08-05/11)- Phase 1, **Nanoelectronics Research Institute/Semiconductor Research Corporation (NRI/SRC)**, $525,920 (Total: $873,920 including PSU match of $348,000), (PI with T. Mayer, V. Narayanan, D. Schlom)(40% share)
- Energy Efficient Transistor and Architectures, (06/11 – 12/12) - Phase 1.5, **Nanoelectronics Research Institute/Semiconductor Research Corporation (NRI/SRC) and National Institute of Standards and Technology (NIST)**, $280,000 (PI with T. Mayer)(50% share)

NSF

- Ultra-sensitive Magnetic Sensors Integrating the Giant Magnetoelectric Effect with MEMs and Advanced Microelectronics, (10/08-9/11), **National Science Foundation/Division of Electrical, Communications and Cyber Systems (NSF/ECCS)**, $352,273 (Co-PI with Q. Zhang (PI), EE, PSU and Q. Yang, Radiology, PSU Hershey Medical Center)(50% share)
- EMT/NANO:Co-Exploration of Device and System Architecture for Quantum NanoElectronics," (09/08-08/11), **National Science Foundation/Division of Computing and Communication Foundation (NSF/CCF)**, $200,020 (Co-PI with V. Narayanan (PI), EE, PSU)(50% share)
- Collaborative: Mixed Anion and Cation Based Transistor Architecture for Ultra-Low Power Complementary Logic Applications, (10/10-09/13), **National Science Foundation/ Division of Electrical, Communications and Cyber Systems (NSF/ECCS)**, $472,753 (PI with M. Hudait, EE, Virginia Tech)(50% share)
- MRSEC: Center for Nanoscale Science Supplement titled "Very Low Energy Dissipation Computing using Inter-band Tunneling Injected Non-equilibrium Ballistic Carriers," (10/10-09/13), **National**

Science Foundation/Nanotechnology Research Initiative (NSF/NRI), $300,000, (Co-PI with T. Mayer(PI), EE, PSU)(50% share)

- NERC: NSF Nanosystems Engineering Research Center (NERC) for "Advanced Self-Powered Systems of Integrated Sensors and Technologies (ASSIST)," (10/12 – 09/17), **National Science Foundation,** $18,500,000 **(**Co-PI and Low Power Nanoelectronics Theme Leader)(Candidate's share $425,000)
- EXPEDITION: NSF Expedition in Computing for "Visual Cortex on Silicon," (10/13 – 09/18), **National Science Foundation,** $10,000,000 **(**Low Power Nanoelectronics Theme Leader)(Candidate's share $500,000)
- EFRI 2DARE: Ultra-Low Power, Collective-State Device Technology Based on Electron Correlation in Two-Dimensional Atomic Layers, (9/13 – 12/17), **National Science Foundation,** $2,000,000 **(**Co-PI)(Candidate's share $500,000)
- MRSEC: Center for Nanoscale Science," (10/13-09/16), **National Science Foundation** (NSF), $18,300,000, (Senior Personnel) (Candidate's share $250,000)

DARPA, NSA, ONR, NIST, DTRA, SRC

- Mixed Anion Arsenide-Antimonide Channel Transistors with High-k Gate Stack, (11/09-10/12) **Semiconductor Research Corporation and Defense Advanced Research Projects Agency (SRC/DARPA),** $226,000 (PI)
- Architecture-Device Co-Design for Ultra-Low Power High Performance Design, (10/09-09/11), **National Security Agency (NSA),** $600,000 (Co-PI with V. Narayanan, EE, PSU)(50% share)
- Correlated Electron Switching Based Tunnel Transistors, (7/11-6/15), **Office of Naval Research** (ONR), $1,923,700 (PI with V. Gopalan, R. Engel-Herbert, MSE, PSU, D. Schlom, MSE, Cornell, K. Rabe, Physics, Rutgers)(25% share)
- Development and Demonstration of Next Generation Electronic Warfare Components based on Graphene Technologies, (01/02/12 – 12/31/14), **Office of Naval Research (ONR)**, $1,280,030 (Co-PI with J. Robinson, Electro-optic Center, PSU)(33% share)
- Ultrafast Spectroscopy in Heterojunction Tunnel Transistors, (10/11 – 9/13), **National Institute of Standards and Technology (NIST),** $120,000 (PI)
- Basic Single-Event and Total-Ionizing Dose Mechanisms in Antimony (Sb)-based CMOS Transistors with High-K Dielectric, (4/01/14-3/31/17), **Defense Threat Reduction Agency (DTRA)**, $1,745,560 (PI with D. McMorrow, NRL, K. Saraswat, EE, Stanford U.)(33% share)
- Architecture-Device Co-Design for Ultra-Low Power High Performance Design- Phase 2, (10/12-09/14), **National Security Agency (NSA),** $600,000 (Co-PI with V. Narayanan, EE, PSU)(50% share)

- Center for Low Energy Systems (LEAST) FCRP with Notre Dame Univ. (01/13-12/17) **Semiconductor Research Corporation and Defense Advanced Research Projects Agency (SRC/DARPA)** (total center funding is $ 30,000,000), Candidate is PI and Theme Leader for the "Quantum Engineered Steep Slope Transistors" $ 4,000,000 (over 5 years) (25% share)
- Oxide-based Reconfigurable Single-Electron Logic for Beyond CMOS, (10/13 - 9/14) **(Semiconductor Research Corporation**/Sematech) $62,125 (PI)
- Basic Single-Event and Total-Ionizing Dose Mechanisms in GE/InGaAs-based CMOS Transistors with ALD High-k Dielectric, (09/14 – 08/17) **Defense Threat Reduction Agency (DTRA)**, $1,045,560 (PI with C. Cress, NRL, K. Saraswat, EE, Stanford U.)(33% share)
- Landau FET Using Mott Hubbard Phase Transition, (1/14 - 12/16) **(Semiconductor Research Corporation**) $300,000 (PI)
- Ferroelectric Field Effect Transistor with Steep Switching Slope and Non-Volatile Functionality, (1/16 – 12/18) **(Semiconductor Research Corporation**) $300,000 (PI)
- Orbital Ordering Driven Threshold Switches for Select Devices in 3D X-Point Memories (11/15 – 10/17) **Semiconductor Research Corporation and Defense Advanced Research Projects Agency (SRC/DARPA)** $ 500,000 (PI with S. Gupta, Penn St, and S. Guha, University of Chicago)(50% share)

Industry

- Compound Semiconductor Based Heterojunction Tunnel Transistors for Ultra Low Power Logic Applications-Phase 2, (09/01/09-08/31/12), **Intel Corporation**, $255,000 (PI)
- Ultra-Low Resistance Ohmic Contacts for III-V Digital Logic, (04/01/09-05/01/11), **Intel Corporation**, $250,000 (Co-PI with S. Mohney, Mat. Sc., PSU)(50% share)
- Post CMOS circuits and architecture, (10/01/10-09/30/13), **Academic Research Office (ARO), Intel Corporation**, $170,000 (PI)
- Sub-0.4V Logic Circuits with Steep Sub-threshold Slope Inter-band Tunnel FETs-Phase 2, (06/09-06/11) **Intel Corporation**, $70,000 (PI)
- Supply voltage scalability of III-V based heterojunction tunnel transistors -Phase 1, (09/08-08/09), **Intel Corporation**, $85,000 (PI)
- Multi-Gate III-V QWFET , (3/1/11-2/28/14), **Global Foundries**, $165,000 (PI)
- Germanium and III-V Devices, (08/11 – 07/12), **Applied Materials (AMAT)**, $ 60,000 (PI)
- Ultra Low Resistivity Metal Insulator Semiconductor (MIS) Contacts, (10/12 – 09/13), **Applied Materials** (AMAT), $ 60,000 (PI)
- Reliability Assessment of Highly Scaled High-k Gate Stacks, (10/12 – 09/13**), Applied Materials** (AMAT), $ 60,000 (PI)
- Variation Study of 3D Transistors, (10/11 – 09/14), **Lam Research**, $ 75,000 (PI)
- III-V-based Nanowire MOSFET and NanoPillar Tunnel FET for Ultra Low-Power Nanoelectronics, (2/12 – 07/15), **Samsung GRO**, $ 240,000 (PI)

- Ultra-scaled III-V FinFETs for Next Generation Nanoelectronics (11/15 – 10/16), **Samsung Electronics**, $ 120,000 (PI)
- 5nm Node Logic Transistor Option for Mobile System on a Chip ("SOC") (2/16 – 1/17), **Qualcomm**, $ 50,000 (PI)

Research Supervision (current)

Postdoctoral Researcher (2)

- Ramkrishna Ghosh, PhD, Indian Institute of Science, IISc, Bangalore, India
- Pankaj Sharma, PhD, EPFL, Lausanne, Switzerland

Doctoral Students (5)

1. Nikhil Shukla: Computing with Correlated Electron Devices (Start Date: 01/2013)
2. Himanshu Madan: Graphene RF Integrated Circuits (Start Date: 09/2011)

3. Mike Barth: Antimonide based Low Power Nanoelectronics (Start Date: 09/2011)

4. Rahul Pandey: Electrical Noise in Emerging Devices (Start Date: 01/2013)

5. Matt Jerry: Nanoscale Spatially Resolved Imaging of Correlated Oxide (Start Date: 08/2013)

6. Benjamin Grisafe: Phase Transitions in Two-Dimensional Crystals (Start Date: 01/01/2016)

7. Jeff Smith: Extremely Scaled CMOS and non CMOS Transistors (Start Date: 01/01/2016)

MS Students (0)

None

Graduated Students (16 PhDs, 4 Postdoctoral Researchers, 7 Masters)

1. Tanmoy Maiti (Postdoctoral Associate) (08/09-08/10) (Currently, Assistant Professor at Indian Institute of Technology, Kanpur, India)

2. Ramakrishnan Krishnan, PhD, 12/2009: Reliability Effects Of Soft Errors and NBTI in Current and Emerging Digital Circuits (Currently, Senior Staff Engineer, Advanced Technology Platforms Group, Taiwan Semiconductor and Manufacturing Corp (TSMC), Hsinchu, Taiwan)

3. Saurabh Mookerjea, PhD, 08/2010: Simulation, Design and Fabrication of Tunnel Transistors with steep sub-threshold slopes (Currently, Senior Device Engineer, Logic Technology Development, Intel Corporation, Hillsboro, Oregon)

4. Wei-Chieh Kao, MS (Thesis), 05/2010: Impact of Non-ideal Interfaces on Transistor Performance (Currently, PhD student at Arizona State University)

5. Vikram Sampat Kumar, MS (Thesis), 04/15/2010: An FPGA-based Real Time Tracking For Indoor Environment

6. Srijith Rajamohan, MS (Thesis), 04/2010: A Neural Network based Classifier on the Cell Broadband Engine

7. Ashkar Ali, MS (Thesis), 03/2009: Transport in Silicon Quantum Dots Embedded in a Rare Earth Oxide

8. Chad Ostrowski, BS (Honor's Thesis) 12/2009: Analytical Modeling of Tunnel Diodes

9. Vinay Saripalli, PhD, 10/31/11: Device Architecture Co-Design for Ultra Low Power Logic Using Emerging Tunneling Based Devices (Currently Senior CAD Engineer, Intel Corporation, Santa Clara)

10. Zhao Feng, PhD, 08/31/2011 : Ultra Sensitive Magnetic Sensors Integrating the Giant Magnetoelectric Effect with MEMS and Advanced CMOS (Currently Design Engineer, Texas Instruments, DallaS)
11. Salil Mujumdar, MS (Thesis), 05/2011: Strain Engineering in Nanoscale Transistors (Thesis option) (Current Device Engineer, Inter Molecular Foundry, San Jose)
12. Ashish Agrawal, MS (Thesis), 05/201l: Noise measurement and modeling of nanoscale devices (Thesis option) (Currently Ph.D. candidate at Penn State)
13. Ashkar Ali, PhD, 06/2012: Design and Fabrication of Ultra-low power and High Performance Quantum-well Transistors (IBM PhD Fellow 2010-2011, Currently Senior Device Engineer at Intel Corporation)
14. Feng Li, PhD, 08/2012: Ultra-sensitive Chip-Scale Magnetometers (Currently Design Engineer, Freescale Semiconductors)
15. Srinidhi Kestur, PhD, 01/2012: Accelerating computationally intensive applications using Reconfigurable systems (Currently Senior Design Engineer, Intel Corporation)
16. Euichul Hwang, PhD, 09/2012: Multi-gate III-V Metal Oxide Semiconductor FETs (Currently Device Engineer, Samsung Advanced Institute of Technology, SAIT)
17. Dheeraj Mohata, PhD, 01/2013: Arsenide-Antimonide Hetero-Junction Transistors for Low Power Logic Applications (Currently Integration Engineer, RF Micro Devices)
18. Ayan Kar, Post Doctoral Researcher, 02/13: (Currently Senior Device Engineer, Intel Corporation)

19. Eugene Freeman, MS (Thesis), 11/13: Correlated Electron Based Switches (Currently PhD student at Penn State)

20. Bijesh Rajamohanan: PhD, 05/2014: Fabrication, Characterization and Physics of III-V Tunneling Field Effect Transistors for Low Power Logic and RF Applications (Currently Senior Device Engineer, Sandisk Corporation)

21. Lu Liu: PhD, 05/2014: Classical and Coulomb Blockade III-V Multi-Gate Quantum Well Field Effect Transistors for Ultra Low Power Logic Applications (Currently Senior Device Engineer, Intel Corporation)

22. Ashish Agrawal: PhD, 12/2014: Physics and Technology of Strained Germanium Quantum Well FinFET for Low Power P-Channel Application (Currently Senior Device Engineer, Intel Corporation)

23. Huichu Liu: PhD, 5/2014: Circuit-Device Interaction for Steep Switching Slope Devices (Currently Senior Architecture Engineer, Intel Corporation)

24. Matt Hollander: PhD, 11/2015: Two-Dimensional Materials for Novel Elecctronic Applications: The Graphene Mixer and TaS_2 Hyper FET (Currently Senior Device Engineer, Micron Corporation)

25. Arun VT: PhD, 7/2015: Physics and technology of nanoscale III-V field effect transistors for low power electronics (Currently Senior Device Engineer, Intel Corporation)

26. Nidhi Agrawal: PhD, 7/2015: Numerical Simulation of Variation in 3D NonSilicon Transistors (Currently Senior Reliability Engineer, Micron Corporation)

27. Ali Razavieh (Post Doctoral Associate, PhD, Purdue University, West Lafayette, Indiana)

28. Bikas Das (Post Doctoral Associate, PhD, Indian Association of Cultivation of Science, Kolkata, India)

29. Sandeepan Das Gupta (Post Doctoral Asssociate, PhD. Vanderbilt University)(Currently Senior Device Engineer, Micron Corporation)

30. Himanshu Madan: PhD, 12/2015: RF Electronics based on Emerging Devices (Currently Senior Device Engineer, Intel Corporation)

Publications

Book Chapters

[1] V. Saripalli, V. Narayanan and S. Datta, “Ultra Low Energy Binary Diagram Circuits Using Few Electron Transistors”, *Lecture Notes of the Institute for Computer Sciences, Social Informatics and Telecommunications Engineering*, Springer Berlin Heidelberg, October 2009

[2] V. Eachempati, R. Das, V. Narayanan, Y. Xie, S. Datta and C. Das, “HeTERO: Hybrid Topology Exploration for RF based On Chip Networks”, *Communication Architectures for System-on-Chip (SoC),* CRC Press, September 2010

[3] S. Datta, D. Schlom, “Gate Oxides beyond SiO2”, *Multifunctional Oxide Heterostructures*, Oxford University Press, September 2010

[4] S. Datta, “III-V MOSFETs”, *Future Intelligent Integrated Systems: New Paths to Augmented Silicon CMOS Technologies*, WSPC-Pan Stanford (Singapore), January 2013

[5] Nikhil Shukla, S. Datta, A. Parihar, A. Raychowdhury, “Computing with Relaxation Oscillators*”, Future Trends in Microelectronics*, Wiley, March 2016

Journal Articles

[100] K. Martens, J. W. Jeong, N. Aetukuri, C. Rettner, N. Shukla, E. Freeman, D. N. Esfahani, F. M. Peeters, T. Topuria, P. M. Rice, A. Volodin, B. Douhard, W. Vandervorst, M. G. Samant, S. Datta, and S. S. P. Parkin, "Field Effectand Strongly Localized Carriers in the Metal-Insulator Transition Material VO2", Physical Review Letters, Nov 6, 2015.

[99] H. Paik, J. A. Moyer, T. Spila, J.W. Tashman, J. A. Mundy, E. Freeman, N.Shukla, J.M. Lapano, R. Engel-Herbert, W. Zander, J. Schubert, D.A. Muller, S. Datta, P. Schiffer, and D. G. Schlom, "Transport properties of ultra-thin VO2 films on (001) TiO2 grown by reactive molecular-beam epitaxy" Applied Physics Letters 106, 163101, Oct 19, 2015.

[98] Y. X. Zheng, A. Agrawal, G. B. Rayner, Jr., M. J. Barth, K. Ahmed, S. Datta, and R. Engel-Herbert "In Situ Process Control of Trilayer Gate-Stacks on p-Germanium With 0.85-nm EOT", IEEE Electron Device lett., vol. 36, no. 9, pp 881-883, Sep. 2015

[97] J. U. Mehta, W. A. Borders, H. Liu, R. Pandey, S. Datta, and L. Lunardi, "III–V Tunnel FET Model With Closed-Form Analytical Solution", IEEE Trans. Elec. Dev., vol. , no. , pp , Sept. 2015.

[96] P. Maffezzoni, L. Daniel, N. Shukla, S. Datta, A. Raychowdhury, "Modeling and Simulation of Vanadium Dioxide Relaxation Oscillators", IEEE Trans. Circuits and Systems, vol. 62, no. 9, pp 2207-2215, Sept. 2015.

[95] P. Maffezzoni, L. Daniel, N. Shukla, S. Datta, A. Raychowdhury and V. Narayanan, "Modelling hysteresis in vanadium dioxide oscillators", IET Electron. Lett., vol. 51, pp 819-820, May 2015.

[94] S. Dasgupta, A. Rajashekhar, K. Majumdar, N. Agrawal, A. Razavieh, S. Trolier-Mckinstry, and S. Datta, "Sub-kT/q Switching in Strong Inversion in PbZr0:52Ti0:48O3 Gated Negative Capacitance FETs", IEEE J. Exploratory Solid-State Comp. Dev. and Cir., vol. 1, pp 43-48, Aug. 2015.

[93] N. Shukla, A. V. Thathachary, A. Agrawal, H. Paik, A. Aziz, D. G. Schlom, S. K. Gupta, R. Engel-Herbert and S. Datta, "A steep-slope transistor based on abrupt electronic phase transition", Nature Comm., vol. 6, pp 7812, Jun. 2015.

[92] Y.-C. Lin, R. K. Ghosh, R. Addou, N. Lu, S. M. Eichfeld, H. Zhu, M.-Y. Li, X. Peng, M. J. Kim, L.-J. Li, R. M. Wallace, S. Datta, and J. A. Robinson, "Atomically thin resonant tunnel diodes built from synthetic van der Waals heterostructures", Nature Comm., vol. 6, pp 7311, Jun. 2015.

[91] N. Agrawal, H. Liu, R. Arghavani, V. Narayanan, and S. Datta,, "Impact of Variation in Nanoscale Silicon and Non-Silicon FinFETs and Tunnel FETs on Device and SRAM Performance", IEEE Trans. Electron Devices, vol. 62, no. 6, pp 1691-1697, Jun. 2015.

[90] L. Liu, X. Li, V. Narayanan, and S. Datta,, "A Reconfigurable Low-Power BDD Logic Architecture Using Ferroelectric Single-Electron Transistors", IEEE Trans. Electron Devices, vol. 62, no. 3, pp 1052-1057, Mar. 2015.

[89] A. Parihar, N. Shukla, S. Datta, A. Raychowdhury, "Synchronization of pairwise-coupled, identical, relaxation oscillators based on metal-insulator phase transition devices: A Model Study", J. Appl. Phys. vol. 117, pp 054902 Feb. 2015

[88] M. J. Hollander, Y. Liu, W-J. Lu, L-J. Li, Y-P. Sun, J. A. Robinson, and S. Datta, "Electrically Driven Reversible Insulator–Metal Phase Transition in 1T-TaS2", NanoLetters 15(3), pp 1861-1866, Jan. 2015

[87] Himanshu Madan *, Matthew Jerry*, Alexej Pogrebnyakov , Theresa Mayer , and Suman Datta, “Quantitative Mapping of Phase Coexistence in Mott-Peierls Insulator during Electronic and Thermally Driven Phase Transition”, *ACS Nano*, 9 (2), pp 2009–2017, January 2015 (First and second authors supervised by the candidate)

[86] A. V. Thathachary*, G. Lavallee, M. Cantoro, K. K. Bhuwalka, Y.C. Yeo, S. Maeda and S. Datta, “Impact of Sidewall Passivation and Channel Composition on $In_xGa_{1-x}As$ FinFET

Performance", *IEEE Electron Device Letters*, vol 36, no 2, pp 117, February 2015 (First author supervised by the candidate)

[85] N. Agrawal*, A. V. Thathachary*, S. Mahapatra and S. Datta, "Impact of Varying Indium(x) Concentration and Quantum Confinement on PBTI Reliability in $In_xGa_{1-x}As$ FinFET", *IEEE Electron Device Letters*, vol 36, no 2, pp 120, January 2015 (First and second authors supervised by the candidate)

[84] Bijesh Rajamohanan*, Rahul Pandey*, Varistha Chobpattana, Canute Vaz, David Gundlach, Kin P. Cheung, John Suehle, Susanne Stemmer, and Suman Datta, "0.5 V Supply Voltage Operation of In0.65Ga0.35As/GaAs0.4Sb0.6 Tunnel FET", *IEEE Electron Device Letters*, vol 36, no 1, pp January 2015 (First and second authors supervised by the candidate)

[83] M. Barth*, G. B. Rayner, S McDonnell, R.M. Wallace, B.R. Bennett, R. Engel-Herbert, and S. Datta "High quality HfO2/p-GaSb(001) metal-oxide-semiconductor capacitors with 0.8nm equivalent oxide thickness", *Applied Physics Letters*, 105, pp 222103, Dec 2, 2014 (First author supervised by the candidate)

[82] Abhinav Parihar, Nikhil Shukla, Suman Datta, and Arijit Raychowdhury, "Exploiting Synchronization Properties of Correlated Electron Devices in a Non-Boolean Computing Fabric for Template Matching", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol4, no 4, pp 400-411, December 2014 (Second author supervised by the candidate)

[81] Yu-Chuan Lin, Chih-Yuan S. Chang, Ram Krishna Ghosh*, Jie Li,§ Hui Zhu, Rafik Addou, Bogdan Diaconescu, Taisuke Ohta, Xin Peng, Ning Lu, Moon J. Kim, Jeremy T. Robinson, Robert M Wallace, Theresa S. Mayer, Suman Datta, Lain-Jong Li, and Joshua A. Robinson, "Atomically Thin Heterostructures Based on Single-Layer Tungsten Diselenide and Graphene", *Nano Letters*, vol 14, pp 6936-6941 November 2014 (Third author supervised by the candidate)

[80] W. Li, Q. Zhang, R. Bijesh*, O.A. Kirillov, Y. Liang, I. Levin, Lian-Mao Peng, C. A. Richter, X. Liang, S. Datta, D. J. Gundlach, and N. V. Nguyen "Electron and hole photoemission detection for band offset determination of tunnel field-effect transistor heterojunctions", *Applied Physics Letters* 105, 213501, November 10, 2014 (Third author supervised by the candidate)

[79] M. S. Kim, H. Liu*, X. Li, S. Datta, and V. Narayanan, "A Steep-Slope Tunnel FET Based SAR Analog-to-Digital Converter", *IEEE Transactions on Electron Devices*, vol. 61, no.11, pp: 3661-3666, November 2014 (Second author supervised by the candidate)

[78] X. Li, H. Liu*, S. Datta, R. Vaddi, V.Narayanan, K. Ma, “Tunnel FET RF Rectifier Design for Energy Harvesting Application”, *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol 4, no 4, pp 400-411, October 2014 (Second author supervised by the candidate)

[77] A. R. Trivedi, S. Datta, and S. Mukhopadhyay "Application of Silicon-Germanium Source Tunnel-FET to Enable Ultralow Power Cellular Neural Network-Based Associative Memory", *IEEE Transactions on Electron Devices*, vol. 61, no.11, pp 3707-3715, November 2014 (equal contribution by all authors)

[76] M. Huefner, R. Ghosh*, E. Freeman*, N. Shulka*, H. Paik, D. G. Schlom, and S. Datta "Hubbard Gap Modulation in Vanadium Dioxide Nanoscale Tunnel Junctions", *Nano Letters*, vol 14, no 11, pp 6115-6120, September 2014 (Second, third and fourth authors supervised by the candidate)

[75] A. Agrawal*, M. Barth*, H. Madan*, Yi-Jing Lee, You-Ru Lin, Cheng-Hsien Wu, Chih-Hsin Ko, C. H. Wann, D. Loubychev, A. Liu, J. Fastenau, J. Lindemuth, and S. Datta "Comparative analysis of hole transport in compressively strained InSb and Ge quantum well heterostructures", *Applied Physics Letters* 105, 052102, August 5, 2014 (First, second and third authors supervised by the candidate).

[74] N. Shukla*, T. Joshi, S. Dasgupta*, P. Borisov, D. Lederman, and S. Datta "Electrically induced insulator to metal transition in epitaxial SmNiO3 thin films", *Applied Physics Letters* 105, 012108, July 11, 2014 (First and third authors supervised by the candidate).

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Recent Invited Talks (selected)

Universities

"Steep Slope Phase Transition FETs and their applications" École Polytechnique Fédérale de Lausanne EPFL, Lausanne, Switzerland, 1/2016

"Inter-band Tunnel Transistors: Opportunities and Challenges", *NEEDS Seminar*, Purdue University, West Lafayette, IN, 10/2015

"Negative Capacitance Ferroelectric Transistors: A Promising Steep Slope Device Candidate?", *NEEDS Seminar*, Purdue University, West Lafayette, IN, 10/2015

"Ultra Low Power Devices", *IEEE EDS Distinguished lecture series in Workshop on Connected, Autonomously Powered Systems,* Columbia University, New York, NY, 04/2014

"Cool Device Strategies for Beyond CMOS Nanoelectronics", *ECE Colloquium,* University of Texas, Dallas, TX, 02/2014

"Cool Device Strategies for Beyond CMOS Nanoelectronics", *ECE Colloquium,* Cornell University, Ithaca, NY, 02/2012

"Nanoelectronics for Future Energy Efficient Information Processing", *ECE Colloquium,* University of Illinois, Urbana Champagne, IL, 03/2012

"Tunnel Transistor Based Energy Efficient Logic", *IEEE EDS Distinguished lecture series in Electronics/Photonics,* Ohio State University, Columbus, OH, 04/2010

"Energy Efficient Logic Transistors using Compound Semiconductors" Cornell University Electron Devices Society Lecture Series, Cornell University, Ithaca, NY, 04/2010

"Logic and Memory Design using Inter-band Tunnel Transistor" Nanoseminar Seminar Series, Arizona State University, 03/2010

"Compound Semiconductor based Logic Elements" IEEE Electron Devices Mini Colloquium, Indian Institute of Technology, Mumbai, 01/2010

"Ushering in the Green Transistor Era", Rochester Institute of Technology, Rochester, New York, 5/2009

"Green Transistors to Green Architectures", Institut für Materialien und Bauelemente der Elektronik, Leibniz Universität Hannover (University of Hannover), Hannover, Germany, 10/2009

"Green Nanoelectronic Computing Devices", as part of the annual workshop on Emerging Trends in Photonic and Electronic Device Research held sponsored by The University of Illinois chapters of the Optical Society of America (OSA) and the IEEE Electron Devices Society (EDS) in conjunction with the Micro and Nanotechnology Laboratory (MNTL), University of Illinois, Urbana Champagne, Illinois, 09/2008

"Recent Advances in Silicon and Non-Silicon Nanoelectronic Devices for High-Performance, Energy Efficient Logic Applications", Penn State University Computer Science and Engineering Colloquia Series, 11/2007

"Emerging Nanoelectronic Devices for High-Speed and Ultra-Low Power Applications", sponsored by the University of Wisconsin, Madison, Materials Research Science and Engineering

Center (MRSEC) in association with Electrical Engineering Department University of Wisconsin, Madison, Wisconsin, 12/2006

"Ultra Low Power Nanoelectronics for the Logic technology", Taipei Local Chapter of IEEE Electron Devices Society (EDS), National Tchao-tung University (NCTU), Hsinshu, Taiwan:, 12/2006

"Emerging Nanoelectronic Devices for High-Speed and Ultra-Low Power Application", Electrical Engineering Colloquium, University of Texas, Austin, 3/2006

"Silicon Nano-Transistors and Nanotechnology for High-Performance Logic Applications", sponsored by the IEEE Phoenix Section Components, Packaging, and Manufacturing Technology Society Chapter, & Waves and Devices Chapter, Arizona State University, Tempe, Arizona, 11/2003

Government/Industry

"Steep Slope Transistors", Speaker at the IEEE Rebooting Computing Workshop, Washington DC, 10/12/2015

"Steep Slope Transduction FETs", Invited Speaker at Global Foundries, Malta, New York, 10/21/2015

"Strained Germanium Quantum Well FinFETs", Invited Speaker at Global Foundries, Malta, New York, 09/01/2015

"Steep Slope Transistors", Keynote Speaker at the NSF sponsored "The Workshop for Energy Efficient Computing" Arlington, VA, 04/14/2015

"Function Stacks for Logic and Memory Devices", Invited Speaker at the SEMATECH's 7th International Symposium on Advanced Gate Stack Technology, in Albany, New York, 09/29/2010-10/01/ 2010

"Non silicon logic elements for extreme voltage scaling ", Invited Speaker at the IBM MRC Workshop on III/V Devices IBM Research, Zurich, Switzerland, 09/2010

"Binary Decision Diagram Logic for Single Electron Devices and Tunnel FETs", Invited Speaker at the Nanoelectronics Research Initiative (NRI) sponsored Architecture & Device Benchmarking Workshop, University of Notre Dame, 08/09/2010

"Tunnel Transistors: From Circuits to Architecture", Invited Speaker at the Nanoelectronics Research Initiative (NRI) sponsored Architecture & Device Benchmarking Workshop, University of Notre Dame, 08/09/2010

"High mobility channel MOSFETs: to include or not to include in the ITRS?", Panelist at the Sematech/IMEC III-V Workshop for discussion on inclusion high mobility channel MOSFETs in the ITRS, Hilton Hawaiian Village, Honolulu, 06/2010

"Green Transistors to Green Architectures", Tutorial at the 16th IEEE International Symposium on High-Performance Computer Architecture (HPCA), Bangalore, India, 01/2010

"High Mobility Channel MOSFETs", Panelist at the Workshop for Future III-V Complementary Metal–Oxide–Semiconductor (CMOS) Technology, Washington DC , December 2009

"Heterojunction Tunnel Transistor Logic," Intel on-site NRI sponsored PI's Workshop, Intel Corporation, Portland, Oregon, 8/2009

"Tunnel Transistor Logic", Intel Microprocessor Research Lab Seminar, Portland, Oregon, 10/09

"Looking Beyond Silicon - A Pipe Dream or the Inevitable Next Step?" Panelist on the IEDM sponsored evening panel called (This panel assembled internationally recognized panelists to discuss the future of Complementary Metal-Oxide Semiconductor (CMOS) and beyond CMOS for leading-edge advanced integrated circuit applications", 12/2007

"III-V Complementary Metal-Oxide Semiconductor (CMOS) on Si: Technical and Manufacturing Needs" Panelist on the Sematech and Aixtron sponsored workshop on readiness of III-V MOSFET Technology. This workshop received world-wide press coverage under the heading "III-V Compounds Emerging as Prime Materials for Future NMOS Channels, Technologists Indicate at SEMATECH & AIXTRON Workshop," Washington, D.C., 12/2007

Inventions

[164] US Patent # 9048314 "Field effect transistor with narrow bandgap source and drain regions and method of fabrication"

[163] US Patent # 9006707 "Forming arsenide-based complementary logic on a single substrate"

[162] US Patent # 8841180 "Strain-inducing semiconductor regions"

[161] US Patent # 8816394 "Field effect transistor with narrow bandgap source and drain regions and method of fabrication"

[160] US Patent # 8803255 "Gate electrode having a capping layer "

[159] US Patent # 8802517 "Extreme high mobility CMOS logic "

[158] US Patent # 8664694 "Field effect transistor with narrow bandgap source and drain regions and method of fabrication"

[157] US Patent # 8638591 "TFET based 4T memory devices"

[156] US Patent # 8581258 "Semiconductor device structures and methods of forming semiconductor structures"

[155] US Patent # 8530884 "Strain inducing semiconductor regions"

[154] US Patent # 8518768 "Extreme high mobility CMOS logic"

[153] US Patent # 8421059 "Strain inducing semiconductor region"

[152] US Patent # 8405164 "Tri-gate transistor device with stress incorporation layer and method of fabrication "

[151] US Patent # 8390082 "Gate electrode having a capping layer "

[150] US Patent # 8369134 "TFET based 6T SRAM cell "

[149] US Patent # 8368135 "Field effect transistor with narrow bandgap source and drain regions and method of fabrication"

[148] US Patent # 8294180 "CMOS devices with a single work function gate electrode and method of fabrication"

[147] US Patent # 8288233 "Method to introduce uniaxial strain in multigate nanoscale transistors by self aligned SI to SIGE conversion processes and structures formed thereby "

[146] US Patent # 8273626 "Nonplanar semiconductor device with partially or fully wrapped around gate electrode and methods of fabrication"

[145] US Patent # 8264004 "Mechanism for forming a remote delta doping layer of a quantum well structure"

[144] US Patent # 8237234 "Transistor gate electrode having conductor material layer"

[143] US Patent # 8232588 "Increasing the surface area of a memory cell capacitor"

[142] US Patent # 8217383 "High hole mobility p-channel Ge transistor structure on Si substrate"

[141] US Patent # 8193567 "Process for integrating planar and non-planar CMOS transistors on a bulk substrate and article made thereby "

[140] US Patent # 8183646 "Field effect transistor with narrow bandgap source and drain regions and method of fabrication "

[139] US Patent # 8183556 "Extreme high mobility CMOS logic"

[138] US Patent # 8169027 "Substrate band gap engineered multi-gate pMOS devices"

[137] US Patent # 8148786 “Complementary metal oxide semiconductor integrated circuit using raised source drain and replacement metal gates”

[136] US Patent # 8138042 “Capacitor, method of increasing a capacitance area of same, and system containing same”

[135] US Patent # 8129795 “Inducing strain in the channels of metal gate transistors”

[134] US Patent # 8124959 “High hole mobility semiconductor device”

[133] US Patent # 8120065 “Tensile strained NMOS transistor using group III-N source/drain regions”

[132] US Patent # 8119508 “Forming integrated circuits with replacement metal gate electrodes”

[131] US Patent # 8084818 “High mobility tri-gate devices and methods of fabrication”

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[127] US Patent # 7960794 “Non-planar pMOS structure with a strained channel region and an integrated strained CMOS flow,” B. Doyle, S. Datta, B. Jin, N. Zelick, R. Chau, June 14, 2011

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[113] US Patent # 7858481 "Method for fabricating transistor with thinned channel," J. Brask, R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, A. Majumdar, M. Metz, M. Radosavljevic, Dec 28, 2010

[112] US Patent # 7825481 “Field effect transistor with narrow bandgap source and drain regions and method of fabrication,” R. Chau, S. Datta, J. Kavalieros, J. Brask, M. Doczy, M. Metz, Nov 02, 2010

[111] US Patent # 7825437 “Unity beta ratio tri-gate transistor static random access memory (SRAM),” R. Pillarisetty, S. Datta, J. Kavalieros, B. Doyle, U. Shah, Nov 02, 2010

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[97] US Patent # 7671471 "Method for making a semiconductor device having a high-k dielectric layer and a metal gate electrode," J. Brask, J. Kavalieros, M. Doczy, U. Shah, C. Barnes, M. Metz, S. Datta, A. Cappellani, R. Chau, March 03, 2010.

[96] US Patent # 7642610 "Transistor gate electrode having conductor material layer," A. Murthy, B. Boyanov, S. Datta, B. Doyle, B. Jin, S. Yu, R. Chau, January 05, 2010.

[95] US Patent # 7642603 "Semiconductor device with reduced fringe capacitance," S. Datta, T. Rakshit, J. Kavalieros, B. Doyle, January 05, 2010.

[94] US Patent # 7638169 "Directing carbon nanotube growth," M. Radosavljevic, J. Kavalieros, A. Majumdar, S. Datta, December 29, 2009.

[93] US Patent # 7629643 "Independent n-tips for multi-gate transistors," R. Pillarisetty, S. Datta, J. Kavalieros, B. Doyle, December 12, 2009

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[87] US Patent # 7575991 "Removing a high-k gate dielectric," M. Doczy, R. Norman, J. Brask, M. Metz, S. Datta, R. Chau, August 18, 2009.

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[83] US Patent # 7560756 "Tri-gate devices and methods of fabrication," R. Chau, B. Doyle, J. Kavalieros, D. Barlage, S. Datta, July 14, 2009.

[82] US Patent # 7547637 "Methods for patterning a semiconductor film," J. Brask, J. Kavalieros, U. Shah, S. Datta, A. Majumdar, R. Chau, B. Doyle, June 16, 2009.

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[80] US Patent # 7531404 "Semiconductor device having a metal gate electrode formed on an annealed high-k gate dielectric layer," S. Pae, J. Maiz, J. Brask, G. Dewey, J. Kavalieros, R. Chau, S. Datta, May 12, 2009.

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Professional Activities

Distinguished Lecturer, Electron Devices Society, IEEE

Fellow, IEEE

Member, *Executive Committee, Electronics and Photonics Division, the Electrochemical Society (ECS)*, September 2009-present

Member, *Executive Committee, Mid-West Institute for Nanoelectronics Discovery (MIND)*, 2008-2012

Member, *Executive Committee, Center for Low Energy Systems Technology (LEAST)*, 2013-present

Member, *"Front End Processes" Tab and contributor to the 2003 Version of the International Technology Roadmap for Semiconductors (ITRS)*

Member, *American Society for Engineering Education*, 2007 – Present

Vice Chair, *Short Course, IEEE International Electron Devices Meeting (IEDM '15)*, Washington DC, December 2016

Chair, *Publications, IEEE International Electron Devices Meeting (IEDM '15)*, Washington DC, December 2015

TPC Member, Design Automation Conference (DAC '16), San Francisco

TPC Member, International Conference on Simulation of Semiconductor Processes & Devices (SISPAD '16), Dresden, Germany

TPC Member, International Reliability Physics Symposium (IRPS '16)

Chair, *Publicity, IEEE International Electron Devices Meeting (IEDM '14)*, San Francisco, California, December 2014

Chair, *Tutorials, IEEE International Electron Devices Meeting (IEDM '12)*, San Francisco, California, December 2012

General Chair, *IEEE Device Research Conference (DRC)*, Notre Dame University, University Park, PA, June 2013

Program Chair, *IEEE Device Research Conference (DRC)*, Pennsylvania State University, University Park, PA, June 2012

Chair, *Emerging Technologies, IEEE International Electron Devices Meeting (IEDM '11)*, Washington DC, December 2011

TPC Vice-Chair, *IEEE Device Research Conference (DRC)*, University of California, Santa Barbara, CA, June 2011

Chair, *Quantum, Power, and Compound Semiconductor Devices Sub-Committee, IEEE International Electron Devices Meeting (IEDM '10)*, San Francisco, California, December 2010

Organizer and Chair, *Rump Session on Embedded Memory called "Looking for Extra Cache", IEEE Device Research Conference (DRC '10)*, Univ. of Notre Dame, June 2010

Organizer and Chair, *Rump Session on Steep Slope Transistors called "Steep Slope or Slippery Slope"*, *IEEE Device Research Conference (DRC '10)*, Penn State University, June 2009

TPC Member, *IEEE Device Research Conference (DRC '10)*, Univ. of Notre Dame, June 2010

TPC Member, *Electronic Materials Conference (EMC '10)*, Univ. of Notre Dame, June 2010

TPC Member, *Semiconductor Interface Specialist Conference (SISC '10)*, San Diego, California, December2010

TPC Member, *European Solid-State Device Research Conference (ESSDERC '09)*, Seville, Spain, September, 2010

TPC Member, *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED '10)*, Austin, Texas, August 2009

TPC Member, *European Solid-State Device Research Conference (ESSDERC '09)*, Athens, Greece, September, 2009

TPC Member, *Quantum, Power, and Compound Semiconductor Devices, IEEE International Electron Devices Meeting (IEDM '09)*, Baltimore, Maryland, December 7– 9, 2009

TPC Member, *IEEE Device Research Conference (DRC '09)*, Penn State Univ., June 2009

TPC Member, *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED '09)*, San Francisco, California, August 2009

TPC Member, *European Solid-State Device Research Conference (ESSDERC '09)*, Edinburgh, Scotland, September 2008

TPC Member, *Silicon Nanoelectronics Workshop (SNW '08)*, Honolulu, Hawaii, June 2008

TPC Member, *International Symposium on VLSI Technology, Systems, and Applications (2005 IEEE VLSI-TSA)*, Hinshu, Taiwan, April 25-27, 2005

Arrangements Chair, IEEE *Device Research Conference (DRC)*, Penn State University, June 2009

Panel Chair, *ACM/IEEE International Symposium Low Power Electronics and Design (ISLPED '09)*, San Francisco, California, August 2009

Session Chair, *"Non Volatile Memory" at the High-K Dielectric Materials and Gate Stack Symposium, Electrochemical Society Meeting (ECS '09)*, Vienna, Austria, October 2009

Session Chair, *"MOS Devices" at the IEEE Device Research Conference (DRC '09), June 2009*

Session Chair, *"MOS Devices" at the IEEE Device Research Conference (DRC '09), June 2009*

Session Co-Chair, "III-V Logic Transistors with Advanced Gate Stack" at the *IEEE International Electron Devices Meeting (IEDM '09)*, Baltimore, Maryland, December 8, 2009

Session Co-Chair, *"Heterostructure High-Speed Devices"* at the *IEEE International Electron Devices Meeting (IEDM '08),* San Francisco, California, December 2008

Session Chair, *"Materials for Ge and Si devices"* at the *International Conference on Insulating Films on Semiconductors (INFOS '07),* Athens, Greece, June 2007

NSF Review Panelist- In EPDT, EMT programs in years 2008-2010

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