

## **Suman Datta**

Chang Family Chair Professor of Engineering Innovation

Department of Electrical Engineering

University of Notre Dame

271 Fitzpatrick Hall, Notre Dame, IN 46556

Phone: 574-631-8835 (fax: 574-631-4393)

E-mail: [sdatta@nd.edu](mailto:sdatta@nd.edu); Lab website: <http://www.ndcl.ee.psu.edu/>

### **Education**

PhD, Electrical and Computer Engineering Dept., University of Cincinnati, OH, September 1999

Bachelors, Electrical Engineering Dept., Indian Institute of Technology, Kanpur, India, June 1995

### **Experience**

Chair Professor (2015 – Present)

Department of Electrical Engineering, University of Notre Dame, IN

Professor (2011 – 2015)

Department of Electrical Engineering, Penn State University, PA

Monkowski Associate Professor (Career Development Professorship) (2007-2011)

Department of Electrical Engineering, Penn State University, PA

Principal Engineer (2005-2007)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Senior Staff Engineer (2003-2005)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Staff Engineer (2002-2003)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Senior Process Engineer (1999-2002)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Technology CAD (TCAD) Engineer (1999)

Avanti Corporation (now Synopsis), Fremont, CA

Technology Consultant for TSMC (Taiwan Semiconductor Manufacturing Corp), UMC (United

Microelectronics Corp) and Samsung Electronics (2008 – Present)

### **Research Grants**

Funding to date (Candidate's share = \$8,102,354):

– 1 NRI grant (The Midwest Institute for Nanoelectronics Discovery: Energy Efficient Transistor and Architecture Center (2007-2012)

– 8 NSF grants (including premier Research Centers like i) Nanosystem Engineering Research Center (NERC) for Advanced Self Powered Systems of Integrated Sensors and Technologies; ii)

Expedition in Computing for Visual Cortex on Silicon; iii) Center for Nanoscale Science – MRSEC center; iv) Emerging Frontiers in Research and Innovation 2014 (EFRI-2014) on Two-Dimensional Atomic-layer Research and Engineering (2-DARE))

- 3 DARPA/SRC grants (Center for Low Energy Systems, LEAST FCRP, at Notre Dame; Materials, Structures and Devices (MARCO MSD Center) at MIT)
- 2 ONR, 2 DTRA, 1 NIST and 2 NSA grants
- 13 Industry grants (including Fortune 500 companies like Intel, Samsung, TSMC, Lam Research, Applied Materials, Global Foundries, Qualcomm)

Total number of publications to date:

- 212 total (100 journal, 112 refereed conferences)
- h-index = 45 with 7,113 citations (Google Scholar)

Total number of graduate students to date:

Postdoctoral: **5 completed, 1 current**

PhD: **17 graduated, 6 current** (including 2 IBM PhD Fellows, 1 Lam research PhD Fellow);

MS: **7 graduated** (with thesis option), 0 current

Total number of issued United States patents: **165**

## Current Research Interests

- Extending CMOS (e.g. germanium, compound semiconductor channel FinFETs)
- Beyond CMOS (e.g. tunneling transistors, ferroelectric transistors)
- Millimeter Wave Electronics (e.g. graphene ambipolar mixers and amplifiers)
- Correlated Oxide Electronics (e.g. coupled oscillators, phase transition FETs and RF switches)
- Co-Design of Emerging Devices, Circuits and Architecture (e.g. heterogeneous core processor)
- Neuromorphic or Cognitive Processors (e.g. visual cortex on a chip)
- Energy constrained Computing for Internet-of-Things (IOT) (e.g. non-volatile processors)

## Awards and Honors

- Penn State Engineering Alumni Society (PSEAS) Premier Research Award (2015)
- IEEE Fellow for “contributions to for contributions to high-performance advanced silicon and compound semiconductor transistor technologies” (2013)
- SEMI Award for North America “in recognition of their pioneering work in the development, integration and introduction of a successful high-k dielectric and metal electrode gate stack for 45 nm CMOS IC production” (2012)
- IBM Faculty Award (2012)

- Penn State Engineering Alumni Society (PSEAS) Outstanding Research Award (2012)
- Distinguished Lecturer of IEEE Electron Devices Society (2011)
- Joseph Monkowsky Professorship for Faculty Early Career Development, The Pennsylvania State University (2007)
- Intel Achievement Award (the highest technical honor at Intel) for “developing the world’s first high-K/metal gate CMOS transistors with record-setting performance” (2003)
- Divisional Achievement Award from Intel Logic Technology Development Group for “invention and successful demonstration of high performance Tri-gate CMOS transistors” (2002)
- All India Rank of 124 (Eastern Zone Rank: 18) among 300,000 students who appeared for Indian Institute of Technology Joint Entrance Examination (IIT-JEE) (1995)

## Funded Projects

### NRI

- Energy Efficient Transistor and Architectures, (06/08-05/11)- Phase 1, **Nanoelectronics Research Institute/Semiconductor Research Corporation (NRI/SRC)**, \$525,920 (Total: \$873,920 including PSU match of \$348,000), (PI with T. Mayer, V. Narayanan, D. Schlom)(40% share)
- Energy Efficient Transistor and Architectures, (06/11 – 12/12) - Phase 1.5, **Nanoelectronics Research Institute/Semiconductor Research Corporation (NRI/SRC) and National Institute of Standards and Technology (NIST)**, \$280,000 (PI with T. Mayer)(50% share)

### NSF

- Ultra-sensitive Magnetic Sensors Integrating the Giant Magnetoelectric Effect with MEMs and Advanced Microelectronics, (10/08-9/11), **National Science Foundation/Division of Electrical, Communications and Cyber Systems (NSF/ECCS)**, \$352,273 (Co-PI with Q. Zhang (PI), EE, PSU and Q. Yang, Radiology, PSU Hershey Medical Center)(50% share)
- EMT/NANO:Co-Exploration of Device and System Architecture for Quantum NanoElectronics,” (09/08-08/11), **National Science Foundation/Division of Computing and Communication Foundation (NSF/CCF)**, \$200,020 (Co-PI with V. Narayanan (PI), EE, PSU)(50% share)
- Collaborative: Mixed Anion and Cation Based Transistor Architecture for Ultra-Low Power Complementary Logic Applications, (10/10-09/13), **National Science Foundation/ Division of Electrical, Communications and Cyber Systems (NSF/ECCS)**, \$472,753 (PI with M. Hudait, EE, Virginia Tech)(50% share)
- MRSEC: Center for Nanoscale Science Supplement titled “Very Low Energy Dissipation Computing using Inter-band Tunneling Injected Non-equilibrium Ballistic Carriers,” (10/10-09/13), **National**

**Science Foundation/Nanotechnology Research Initiative** (NSF/NRI), \$300,000, (Co-PI with T. Mayer(PI), EE, PSU)(50% share)

- NERC: NSF Nanosystems Engineering Research Center (NERC) for “Advanced Self-Powered Systems of Integrated Sensors and Technologies (ASSIST),” (10/12 – 09/17), **National Science Foundation**, \$18,500,000 (Co-PI and Low Power Nanoelectronics Theme Leader)(Candidate’s share \$425,000)
- EXPEDITION: NSF Expedition in Computing for “Visual Cortex on Silicon,” (10/13 – 09/18), **National Science Foundation**, \$10,000,000 (Low Power Nanoelectronics Theme Leader)(Candidate’s share \$500,000)
- EFRI 2DARE: Ultra-Low Power, Collective-State Device Technology Based on Electron Correlation in Two-Dimensional Atomic Layers, (9/13 – 12/17), **National Science Foundation**, \$2,000,000 (Co-PI)(Candidate’s share \$500,000)
- MRSEC: Center for Nanoscale Science,” (10/13-09/16), **National Science Foundation** (NSF), \$18,300,000, (Senior Personnel) (Candidate’s share \$250,000)

#### **DARPA, NSA, ONR, NIST, DTRA, SRC**

- Mixed Anion Arsenide-Antimonide Channel Transistors with High-k Gate Stack, (11/09-10/12) **Semiconductor Research Corporation and Defense Advanced Research Projects Agency (SRC/DARPA)**, \$226,000 (PI)
- Architecture-Device Co-Design for Ultra-Low Power High Performance Design, (10/09-09/11), **National Security Agency (NSA)**, \$600,000 (Co-PI with V. Narayanan, EE, PSU)(50% share)
- Correlated Electron Switching Based Tunnel Transistors, (7/11-6/15), **Office of Naval Research** (ONR), \$1,923,700 (PI with V. Gopalan, R. Engel-Herbert, MSE, PSU, D. Schlom, MSE, Cornell, K. Rabe, Physics, Rutgers)(25% share)
- Development and Demonstration of Next Generation Electronic Warfare Components based on Graphene Technologies, (01/02/12 – 12/31/14), **Office of Naval Research (ONR)**, \$1,280,030 (Co-PI with J. Robinson, Electro-optic Center, PSU)(33% share)
- Ultrafast Spectroscopy in Heterojunction Tunnel Transistors, (10/11 – 9/13), **National Institute of Standards and Technology (NIST)**, \$120,000 (PI)
- Basic Single-Event and Total-Ionizing Dose Mechanisms in Antimony (Sb)-based CMOS Transistors with High-K Dielectric, (4/01/14-3/31/17), **Defense Threat Reduction Agency (DTRA)**, \$1,745,560 (PI with D. McMorrow, NRL, K. Saraswat, EE, Stanford U.)(33% share)
- Architecture-Device Co-Design for Ultra-Low Power High Performance Design- Phase 2, (10/12-09/14), **National Security Agency (NSA)**, \$600,000 (Co-PI with V. Narayanan, EE, PSU)(50% share)

- Center for Low Energy Systems (LEAST) FCRP with Notre Dame Univ. (01/13-12/17) **Semiconductor Research Corporation and Defense Advanced Research Projects Agency (SRC/DARPA)** (total center funding is \$ 30,000,000), Candidate is PI and Theme Leader for the “Quantum Engineered Steep Slope Transistors” \$ 4,000,000 (over 5 years) (25% share)
- Oxide-based Reconfigurable Single-Electron Logic for Beyond CMOS, (10/13 - 9/14) **(Semiconductor Research Corporation/Sematech)** \$62,125 (PI)
- Basic Single-Event and Total-Ionizing Dose Mechanisms in GE/InGaAs-based CMOS Transistors with ALD High-k Dielectric, (09/14 – 08/17) **Defense Threat Reduction Agency (DTRA)**, \$1,045,560 (PI with C. Cress, NRL, K. Saraswat, EE, Stanford U.)(33% share)
- Landau FET Using Mott Hubbard Phase Transition, (1/14 - 12/16) **(Semiconductor Research Corporation)** \$300,000 (PI)
- Ferroelectric Field Effect Transistor with Steep Switching Slope and Non-Volatile Functionality, (1/16 – 12/18) **(Semiconductor Research Corporation)** \$300,000 (PI)
- Orbital Ordering Driven Threshold Switches for Select Devices in 3D X-Point Memories (11/15 – 10/17) **Semiconductor Research Corporation and Defense Advanced Research Projects Agency (SRC/DARPA)** \$ 500,000 (PI with S. Gupta, Penn St, and S. Guha, University of Chicago)(50% share)

## Industry

- Compound Semiconductor Based Heterojunction Tunnel Transistors for Ultra Low Power Logic Applications-Phase 2, (09/01/09-08/31/12), **Intel Corporation**, \$255,000 (PI)
- Ultra-Low Resistance Ohmic Contacts for III-V Digital Logic, (04/01/09-05/01/11), **Intel Corporation**, \$250,000 (Co-PI with S. Mohny, Mat. Sc., PSU)(50% share)
- Post CMOS circuits and architecture, (10/01/10-09/30/13), **Academic Research Office (ARO), Intel Corporation**, \$170,000 (PI)
- Sub-0.4V Logic Circuits with Steep Sub-threshold Slope Inter-band Tunnel FETs-Phase 2, (06/09-06/11) **Intel Corporation**, \$70,000 (PI)
- Supply voltage scalability of III-V based heterojunction tunnel transistors -Phase 1, (09/08-08/09), **Intel Corporation**, \$85,000 (PI)
- Multi-Gate III-V QWFET , (3/1/11-2/28/14), **Global Foundries**, \$165,000 (PI)
- Germanium and III-V Devices, (08/11 – 07/12), **Applied Materials (AMAT)**, \$ 60,000 (PI)
- Ultra Low Resistivity Metal Insulator Semiconductor (MIS) Contacts, (10/12 – 09/13), **Applied Materials (AMAT)**, \$ 60,000 (PI)
- Reliability Assessment of Highly Scaled High-k Gate Stacks, (10/12 – 09/13), **Applied Materials (AMAT)**, \$ 60,000 (PI)
- Variation Study of 3D Transistors, (10/11 – 09/14), **Lam Research**, \$ 75,000 (PI)
- III-V-based Nanowire MOSFET and NanoPillar Tunnel FET for Ultra Low-Power Nanoelectronics, (2/12 – 07/15), **Samsung GRO**, \$ 240,000 (PI)

- Ultra-scaled III-V FinFETs for Next Generation Nanoelectronics (11/15 – 10/16), **Samsung Electronics**, \$ 120,000 (PI)
- 5nm Node Logic Transistor Option for Mobile System on a Chip (“SOC”) (2/16 – 1/17), **Qualcomm**, \$ 50,000 (PI)

## **Research Supervision (current)**

### **Postdoctoral Researcher (2)**

- Ramkrishna Ghosh, PhD, Indian Institute of Science, IISc, Bangalore, India
- Pankaj Sharma, PhD, EPFL, Lausanne, Switzerland

### **Doctoral Students (5)**

1. Nikhil Shukla: Computing with Correlated Electron Devices (Start Date: 01/2013)
2. Himanshu Madan: Graphene RF Integrated Circuits (Start Date: 09/2011)
3. Mike Barth: Antimonide based Low Power Nanoelectronics (Start Date: 09/2011)
4. Rahul Pandey: Electrical Noise in Emerging Devices (Start Date: 01/2013)
5. Matt Jerry: Nanoscale Spatially Resolved Imaging of Correlated Oxide (Start Date: 08/2013)
6. Benjamin Grisafe: Phase Transitions in Two-Dimensional Crystals (Start Date: 01/01/2016)
7. Jeff Smith: Extremely Scaled CMOS and non CMOS Transistors (Start Date: 01/01/2016)

### **MS Students (0)**

None

### **Graduated Students (16 PhDs, 4 Postdoctoral Researchers, 7 Masters)**

1. Tanmoy Maiti (Postdoctoral Associate) (08/09-08/10) (Currently, Assistant Professor at Indian Institute of Technology, Kanpur, India)
2. Ramakrishnan Krishnan, PhD, 12/2009: Reliability Effects Of Soft Errors and NBTI in Current and Emerging Digital Circuits (Currently, Senior Staff Engineer, Advanced Technology Platforms Group, Taiwan Semiconductor and Manufacturing Corp (TSMC), Hsinchu, Taiwan)
3. Saurabh Mookerjee, PhD, 08/2010: Simulation, Design and Fabrication of Tunnel Transistors with steep sub-threshold slopes (Currently, Senior Device Engineer, Logic Technology Development, Intel Corporation, Hillsboro, Oregon)

*Last updated, Dec 2015*

4. Wei-Chieh Kao, MS (Thesis), 05/2010: Impact of Non-ideal Interfaces on Transistor Performance (Currently, PhD student at Arizona State University)
5. Vikram Sampat Kumar, MS (Thesis), 04/15/2010: An FPGA-based Real Time Tracking For Indoor Environment
6. Srijith Rajamohan, MS (Thesis), 04/2010: A Neural Network based Classifier on the Cell Broadband Engine
7. Ashkar Ali, MS (Thesis), 03/2009: Transport in Silicon Quantum Dots Embedded in a Rare Earth Oxide
8. Chad Ostrowski, BS (Honor's Thesis) 12/2009: Analytical Modeling of Tunnel Diodes
9. Vinay Saripalli, PhD, 10/31/11: Device Architecture Co-Design for Ultra Low Power Logic Using Emerging Tunneling Based Devices (Currently Senior CAD Engineer, Intel Corporation, Santa Clara)
10. Zhao Feng, PhD, 08/31/2011 : Ultra Sensitive Magnetic Sensors Integrating the Giant Magnetoelectric Effect with MEMS and Advanced CMOS (Currently Design Engineer, Texas Instruments, Dallas)
11. Salil Mujumdar, MS (Thesis), 05/2011: Strain Engineering in Nanoscale Transistors (Thesis option) (Current Device Engineer, Inter Molecular Foundry, San Jose)
12. Ashish Agrawal, MS (Thesis), 05/2011: Noise measurement and modeling of nanoscale devices (Thesis option) (Currently Ph.D. candidate at Penn State)
13. Ashkar Ali, PhD, 06/2012: Design and Fabrication of Ultra-low power and High Performance Quantum-well Transistors (IBM PhD Fellow 2010-2011, Currently Senior Device Engineer at Intel Corporation)
14. Feng Li, PhD, 08/2012: Ultra-sensitive Chip-Scale Magnetometers (Currently Design Engineer, Freescale Semiconductors)
15. Srinidhi Kestur, PhD, 01/2012: Accelerating computationally intensive applications using Reconfigurable systems (Currently Senior Design Engineer, Intel Corporation)
16. Euichul Hwang, PhD, 09/2012: Multi-gate III-V Metal Oxide Semiconductor FETs (Currently Device Engineer, Samsung Advanced Institute of Technology, SAIT)
17. Dheeraj Mohata, PhD, 01/2013: Arsenide-Antimonide Hetero-Junction Transistors for Low Power Logic Applications (Currently Integration Engineer, RF Micro Devices)
18. Ayan Kar, Post Doctoral Researcher, 02/13: (Currently Senior Device Engineer, Intel Corporation)

19. Eugene Freeman, MS (Thesis), 11/13: Correlated Electron Based Switches (Currently PhD student at Penn State)
20. Bijesh Rajamohanan: PhD, 05/2014: Fabrication, Characterization and Physics of III-V Tunneling Field Effect Transistors for Low Power Logic and RF Applications (Currently Senior Device Engineer, Sandisk Corporation)
21. Lu Liu: PhD, 05/2014: Classical and Coulomb Blockade III-V Multi-Gate Quantum Well Field Effect Transistors for Ultra Low Power Logic Applications (Currently Senior Device Engineer, Intel Corporation)
22. Ashish Agrawal: PhD, 12/2014: Physics and Technology of Strained Germanium Quantum Well FinFET for Low Power P-Channel Application (Currently Senior Device Engineer, Intel Corporation)
23. Huichu Liu: PhD, 5/2014: Circuit-Device Interaction for Steep Switching Slope Devices (Currently Senior Architecture Engineer, Intel Corporation)
24. Matt Hollander: PhD, 11/2015: Two-Dimensional Materials for Novel Electronic Applications: The Graphene Mixer and TaS<sub>2</sub> Hyper FET (Currently Senior Device Engineer, Micron Corporation)
25. Arun VT: PhD, 7/2015: Physics and technology of nanoscale III-V field effect transistors for low power electronics (Currently Senior Device Engineer, Intel Corporation)
26. Nidhi Agrawal: PhD, 7/2015: Numerical Simulation of Variation in 3D NonSilicon Transistors (Currently Senior Reliability Engineer, Micron Corporation)
27. Ali Razavieh (Post Doctoral Associate, PhD, Purdue University, West Lafayette, Indiana)
28. Bikas Das (Post Doctoral Associate, PhD, Indian Association of Cultivation of Science, Kolkata, India)
29. Sandeepan Das Gupta (Post Doctoral Associate, PhD, Vanderbilt University )(Currently Senior Device Engineer, Micron Corporation)
30. Himanshu Madan: PhD, 12/2015: RF Electronics based on Emerging Devices (Currently Senior Device Engineer, Intel Corporation)

## **Publications**

### **Book Chapters**



- [1] V. Saripalli, V. Narayanan and S. Datta, "Ultra Low Energy Binary Diagram Circuits Using Few Electron Transistors", *Lecture Notes of the Institute for Computer Sciences, Social Informatics and Telecommunications Engineering*, Springer Berlin Heidelberg, October 2009
- [2] V. Eachempati, R. Das, V. Narayanan, Y. Xie, S. Datta and C. Das, "HeTERO: Hybrid Topology Exploration for RF based On Chip Networks", *Communication Architectures for System-on-Chip (SoC)*, CRC Press, September 2010
- [3] S. Datta, D. Schlom, "Gate Oxides beyond SiO<sub>2</sub>", *Multifunctional Oxide Heterostructures*, Oxford University Press, September 2010
- [4] S. Datta, "III-V MOSFETs", *Future Intelligent Integrated Systems: New Paths to Augmented Silicon CMOS Technologies*, WSPC-Pan Stanford (Singapore), January 2013
- [5] Nikhil Shukla, S. Datta, A. Parihar, A. Raychowdhury, "Computing with Relaxation Oscillators", *Future Trends in Microelectronics*, Wiley, March 2016

#### **Journal Articles**

- [100] K. Martens, J. W. Jeong, N. Aetukuri, C. Rettner, N. Shukla, E. Freeman, D. N. Esfahani, F. M. Peeters, T. Topuria, P. M. Rice, A. Volodin, B. Douhard, W. Vandervorst, M. G. Samant, S. Datta, and S. S. P. Parkin, "Field Effect and Strongly Localized Carriers in the Metal-Insulator Transition Material VO<sub>2</sub>", *Physical Review Letters*, Nov 6, 2015.
- [99] H. Paik, J. A. Moyer, T. Spila, J.W. Tashman, J. A. Mundy, E. Freeman, N. Shukla, J.M. Lapano, R. Engel-Herbert, W. Zander, J. Schubert, D.A. Muller, S. Datta, P. Schiffer, and D. G. Schlom, "Transport properties of ultra-thin VO<sub>2</sub> films on (001) TiO<sub>2</sub> grown by reactive molecular-beam epitaxy" *Applied Physics Letters* 106, 163101, Oct 19, 2015.
- [98] Y. X. Zheng, A. Agrawal, G. B. Rayner, Jr., M. J. Barth, K. Ahmed, S. Datta, and R. Engel-Herbert "In Situ Process Control of Trilayer Gate-Stacks on p-Germanium With 0.85-nm EOT", *IEEE Electron Device Lett.*, vol. 36, no. 9, pp 881-883, Sep. 2015
- [97] J. U. Mehta, W. A. Borders, H. Liu, R. Pandey, S. Datta, and L. Lunardi, "III-V Tunnel FET Model With Closed-Form Analytical Solution", *IEEE Trans. Elec. Dev.*, vol. , no. , pp , Sept. 2015.
- [96] P. Maffezzoni, L. Daniel, N. Shukla, S. Datta, A. Raychowdhury, "Modeling and Simulation of Vanadium Dioxide Relaxation Oscillators", *IEEE Trans. Circuits and Systems*, vol. 62, no. 9, pp 2207-2215, Sept. 2015.

- [95] P. Maffezzoni, L. Daniel, N. Shukla, S. Datta, A. Raychowdhury and V. Narayanan, "Modelling hysteresis in vanadium dioxide oscillators", *IET Electron. Lett.*, vol. 51, pp 819-820, May 2015.
- [94] S. Dasgupta, A. Rajashekhar, K. Majumdar, N. Agrawal, A. Razavieh, S. Trolier-Mckinstry, and S. Datta, "Sub-kT/q Switching in Strong Inversion in PbZr<sub>0.52</sub>Ti<sub>0.48</sub>O<sub>3</sub> Gated Negative Capacitance FETs", *IEEE J. Exploratory Solid-State Comp. Dev. and Cir.*, vol. 1, pp 43-48, Aug. 2015.
- [93] N. Shukla, A. V. Thathachary, A. Agrawal, H. Paik, A. Aziz, D. G. Schlom, S. K. Gupta, R. Engel-Herbert and S. Datta, "A steep-slope transistor based on abrupt electronic phase transition", *Nature Comm.*, vol. 6, pp 7812, Jun. 2015.
- [92] Y.-C. Lin, R. K. Ghosh, R. Addou, N. Lu, S. M. Eichfeld, H. Zhu, M.-Y. Li, X. Peng, M. J. Kim, L.-J. Li, R. M. Wallace, S. Datta, and J. A. Robinson, "Atomically thin resonant tunnel diodes built from synthetic van der Waals heterostructures", *Nature Comm.*, vol. 6, pp 7311, Jun. 2015.
- [91] N. Agrawal, H. Liu, R. Arghavani, V. Narayanan, and S. Datta, "Impact of Variation in Nanoscale Silicon and Non-Silicon FinFETs and Tunnel FETs on Device and SRAM Performance", *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp 1691-1697, Jun. 2015.
- [90] L. Liu, X. Li, V. Narayanan, and S. Datta, "A Reconfigurable Low-Power BDD Logic Architecture Using Ferroelectric Single-Electron Transistors", *IEEE Trans. Electron Devices*, vol. 62, no. 3, pp 1052-1057, Mar. 2015.
- [89] A. Parihar, N. Shukla, S. Datta, A. Raychowdhury, "Synchronization of pairwise-coupled, identical, relaxation oscillators based on metal-insulator phase transition devices: A Model Study", *J. Appl. Phys.* vol. 117, pp 054902 Feb. 2015
- [88] M. J. Hollander, Y. Liu, W.-J. Lu, L.-J. Li, Y.-P. Sun, J. A. Robinson, and S. Datta, "Electrically Driven Reversible Insulator–Metal Phase Transition in 1T-TaS<sub>2</sub>", *NanoLetters* 15(3), pp 1861-1866, Jan. 2015
- [87] Himanshu Madan \*, Matthew Jerry\*, Alexej Pogrebnjakov , Theresa Mayer , and Suman Datta, "Quantitative Mapping of Phase Coexistence in Mott-Peierls Insulator during Electronic and Thermally Driven Phase Transition", *ACS Nano*, 9 (2), pp 2009–2017, January 2015 (First and second authors supervised by the candidate)
- [86] A. V. Thathachary\*, G. Lavallee, M. Cantoro, K. K. Bhuiwarka, Y.C. Yeo, S. Maeda and S. Datta, "Impact of Sidewall Passivation and Channel Composition on In<sub>x</sub>Ga<sub>1-x</sub>As FinFET

Performance”, *IEEE Electron Device Letters*, vol 36, no 2, pp 117, February 2015 (First author supervised by the candidate)

[85] N. Agrawal\*, A. V. Thathachary\*, S. Mahapatra and S. Datta, “Impact of Varying Indium(x) Concentration and Quantum Confinement on PBTI Reliability in  $\text{In}_x\text{Ga}_{1-x}\text{As}$  FinFET”, *IEEE Electron Device Letters*, vol 36, no 2, pp 120, January 2015 (First and second authors supervised by the candidate)

[84] Bijesh Rajamohanan\*, Rahul Pandey\*, Varistha Chobpattana, Canute Vaz, David Gundlach, Kin P. Cheung, John Suehle, Susanne Stemmer, and Suman Datta, “0.5 V Supply Voltage Operation of  $\text{In}_{0.65}\text{Ga}_{0.35}\text{As}/\text{GaAs}_{0.4}\text{Sb}_{0.6}$  Tunnel FET”, *IEEE Electron Device Letters*, vol 36, no 1, pp January 2015 (First and second authors supervised by the candidate)

[83] M. Barth\*, G. B. Rayner, S McDonnell, R.M. Wallace, B.R. Bennett, R. Engel-Herbert, and S. Datta "High quality  $\text{HfO}_2/\text{p-GaSb}(001)$  metal-oxide-semiconductor capacitors with 0.8nm equivalent oxide thickness", *Applied Physics Letters*, 105, pp 222103, Dec 2, 2014 (First author supervised by the candidate)

[82] Abhinav Parihar, Nikhil Shukla, Suman Datta, and Arijit Raychowdhury, “Exploiting Synchronization Properties of Correlated Electron Devices in a Non-Boolean Computing Fabric for Template Matching”, *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol4, no 4, pp 400-411, December 2014 (Second author supervised by the candidate)

[81] Yu-Chuan Lin, Chih-Yuan S. Chang, Ram Krishna Ghosh\*, Jie Li,§ Hui Zhu, Rafik Addou, Bogdan Diaconescu, Taisuke Ohta, Xin Peng, Ning Lu, Moon J. Kim, Jeremy T. Robinson, Robert M Wallace, Theresa S. Mayer, Suman Datta, Lain-Jong Li, and Joshua A. Robinson, “Atomically Thin Heterostructures Based on Single-Layer Tungsten Diselenide and Graphene”, *Nano Letters*, vol 14, pp 6936-6941 November 2014 ( Third author supervised by the candidate)

[80] W. Li, Q. Zhang, R. Bijesh\*, O.A. Kirillov, Y. Liang, I. Levin, Lian-Mao Peng, C. A. Richter, X. Liang, S. Datta, D. J. Gundlach, and N. V. Nguyen "Electron and hole photoemission detection for band offset determination of tunnel field-effect transistor heterojunctions", *Applied Physics Letters* 105, 213501, November 10, 2014 (Third author supervised by the candidate)

[79] M. S. Kim, H. Liu\*, X. Li, S. Datta, and V. Narayanan, "A Steep-Slope Tunnel FET Based SAR Analog-to-Digital Converter", *IEEE Transactions on Electron Devices*, vol. 61, no.11, pp: 3661-3666, November 2014 (Second author supervised by the candidate)

- [78] X. Li, H. Liu\*, S. Datta, R. Vaddi, V.Narayanan, K. Ma, "Tunnel FET RF Rectifier Design for Energy Harvesting Application", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol 4, no 4, pp 400-411, October 2014 (Second author supervised by the candidate)
- [77] A. R. Trivedi, S. Datta, and S. Mukhopadhyay "Application of Silicon-Germanium Source Tunnel-FET to Enable Ultralow Power Cellular Neural Network-Based Associative Memory", *IEEE Transactions on Electron Devices*, vol. 61, no.11, pp 3707-3715, November 2014 (equal contribution by all authors)
- [76] M. Huefner, R. Ghosh\*, E. Freeman\*, N. Shulka\*, H. Paik, D. G. Schlom, and S. Datta "Hubbard Gap Modulation in Vanadium Dioxide Nanoscale Tunnel Junctions", *Nano Letters*, vol 14, no 11, pp 6115-6120, September 2014 (Second, third and fourth authors supervised by the candidate)
- [75] A. Agrawal\*, M. Barth\*, H. Madan\*, Yi-Jing Lee, You-Ru Lin, Cheng-Hsien Wu, Chih-Hsin Ko, C. H. Wann, D. Loubychev, A. Liu, J. Fastenau, J. Lindemuth, and S. Datta "Comparative analysis of hole transport in compressively strained InSb and Ge quantum well heterostructures", *Applied Physics Letters* 105, 052102, August 5, 2014 (First, second and third authors supervised by the candidate).
- [74] N. Shukla\*, T. Joshi, S. Dasgupta\*, P. Borisov, D. Lederman, and S. Datta "Electrically induced insulator to metal transition in epitaxial SmNiO<sub>3</sub> thin films", *Applied Physics Letters* 105, 012108, July 11, 2014 (First and third authors supervised by the candidate).
- [73] H. Liu\*, M. Cotter\*, S. Datta, and V. Narayanan, "Soft-Error Performance Evaluation on Emerging Low Power Devices", *IEEE Transactions on Device and Materials Reliability*, vol. 14, no. 2, June 3, 2014 (First author supervised by the candidate).
- [72] N. Shukla\*, A. Parihar, E. Freeman\*, H. Paik, G. Stone, V. Narayanan, H. Wen, Z. Cai, V. Gopalan, R. Engel-Herbert, D. G. Schlom, A. Raychowdhury, and S. Datta "Synchronized charge oscillations in correlated electron systems", *Nature Scientific Reports* 4:4964, May 14, 2014 (First and third authors supervised by the candidate)
- [71] A. Agrawal\*, J. Lin, M. Barth\*, R.White, B. Zheng, S. Chopra, S. Gupta, K. Wang, J.Gelatos, S. Mohny, and S. Datta "Fermi level depinning and contact resistivity reduction using a reduced titania interlayer in n-silicon metal-insulator-semiconductor ohmic contacts", *Applied Physics Letters* Vol.104, 112101, March 17, 2014 (First and third authors supervised by the candidate).

- [70] M. Hollander\*, H. Madan\*, N. Shukla\*, D. Snyder, J. Robinson, and S. Datta, "Short-channel graphene nanoribbon transistors with enhanced symmetry between p- and n-branches", *Applied Physics Express*, 7, 055103, 2014 (First, second and third authors supervised by the candidate)
- [69] R. Pandey\*, V. Saripalli\*, J.P. Kulkarni, V. Narayanan, and S. Datta, "Impact of Single Trap Random Telegraph Noise on Heterojunction TFET SRAM Stability ", *IEEE Electron Device Letters* Vol. 35. NO. 3, March 2014 (First and second authors supervised by the candidate)
- [68] S Datta, H. Liu\*, and V. Narayana "Tunnel FET technology: A reliability perspective", *Microelectronics Reliability Journal*, March 3, 2014 (Second author supervised by the candidate).
- [67] R. Pandey\*, B. Rajamohanam\*, H. Liu\*, V. Narayanan, and S. Datta, "Electrical Noise in Heterojunction Interband Tunnel FETs", *IEEE Transactions on Electron Devices*, vol. 61, no.2, pp: 552-559, February 2014 (First, second and third authors supervised by the candidate).
- [66] A. V. Thathachary\*, N. Agrawal\*, L. Liu\*, and S. Datta, "Electron Transport in Multigate InxGal-x As Nanowire FETs: From Diffusive to Ballistic Regimes at Room Temperature", *Nano Letters* 14(2):626-33, Feb 2014 (First, second and third authors supervised by the candidate)
- [65] B. Rajamohanam\*, D. Mohata\*, Y. Zhu, M. Hudait, Z. Jiang, M. Hollander\*, G. Klimeck, and S. Datta "Design, fabrication, and analysis of p-channel arsenide/antimonide hetero-junction tunnel transistors" *Journal of Applied Physics* 115, 044502. January 2014 (First, second and sixth authors supervised by the candidate)
- [64] E. Freeman\*, G Stone, N. Shukla\*, H. Paik, J. A. Moyer, Z. Cai, H. Wen, R. Engel-Herbert, D. G. Schlom V. Gopalan, and S. Datta "Nanoscale structural evolution of electrically driven insulator to metal transition in vanadium dioxide", *Applied Physics Letters* Vol.103, Issue 26 December 30, 2013 (First and second authors supervised by the candidate).
- [63] N. Agrawal\*, Y. Kimura, R. Arghavani, and S. Datta, "Impact of Transistor Architecture (Bulk Planar, Trigate on Bulk, Ultrathin-Body Planar SOI) and Material (Silicon or III Semiconductor) on Variation for Logic and SRAM Applications", *IEEE Transactions on Electron Devices*, vol. 60, no.10, pp: 3298-3304, October 2013 (First author supervised by the candidate).
- [62] B. Rajamohanam\*, D. Mohata\*, D. Zhernokletov, B. Brennan, R. M. Wallace, R. Engel-Herbert, and S. Datta, "Low-Temperature Atomic-Layer-Deposited High-k Dielectric for p-Channel In<sub>0.7</sub>Ga<sub>0.3</sub>As/GaAs<sub>0.35</sub>Sb<sub>0.65</sub> Heterojunction Tunneling Field-Effect Transistor", *Applied Physics Express*, 6, 101201, 2013 (First and second authors supervised by the candidate)

- [61] C. Cress and S. Datta, "Nanoscale transistor – Just around the gate", *Science*, vol. 341, pp. 140-141, 2013 (contributed equally by all authors)
- [62] Lubyshev, Joel M. Fastenau, and Amy K. Liu "Structural, morphological, and defect properties of metamorphic  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}/\text{GaAs}_{0.35}\text{Sb}_{0.65}$  p-type tunnel field effect transistor structure grown by molecular beam epitaxy" *Journal of Vacuum Science and Technology B* 31(4), pp 041203-1, Jul/Aug 2013 (Third author supervised by the candidate)
- [61] R. Bijesh\*, D. Mohata\*, A. Ali\*, and Suman Datta "Insight into the output characteristics of III-V tunneling field effect transistors" *Applied Physics Letters* 102, 092105 March 2013 (First, second and third authors supervised by the candidate)
- [60] A Ali\*, H. Madan\*, M. Barth\*, J. B. Boos, B. R. Bennett, and S. Datta "Effect of Interface States on the Performance of Antimonide nMOSFETs" *IEEE Electron Device Letters* Vol. 34. NO. 3, March 2013(first, second and third authors supervised by the candidate)
- [59] YC Chen, S Eachempati, CY Wang, S Datta, Y Xie, V. Narayanan "A Synthesis Algorithm for Reconfigurable Single-Electron Transistor Arrays" *ACM Journal on Emerging Technologies in Computing Systems (JETC)* Volume 9 Issue 1, February 2013 (contributed equally by all authors)
- [58] Ayan Kar\*, Nikhil Shukla\*, Eugene Freeman\*, Hanjong Paik, Huichu Liu\*, Roman Engel-Herbert, S. S. N. Bhardwaja, Darrell G. Schlom, and Suman Datta "Intrinsic electronic switching time in ultrathin epitaxial vanadium dioxide thin film" *Applied Physics Letters* 102, 072106 February 2013 (first, second, third and fifth authors supervised by the candidate)
- [57] L. Liu\*, V. Narayanan, and S.Datta "A programmable ferroelectric single electron transistor" *Appl. Phys. Lett.* 102, 053505 February 2013 (First author supervised by the candidate)
- [56] Y. Zhu, N. Jain, S. Vijayaraghavan, D. K. Mohata\*, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, , and M. K. Hudait "Band offset determination of mixed As/Sb type-II staggered gap heterostructure for n-channel tunnel field effect transistor application" *J. Appl. Phys.* 113, 024319 January 2013 (Fourth author supervised by the candidate)
- [55] S. K. Gupta, J. P Kulkarni, S. Datta and K. Roy, "Heterojunction Intra-band Tunneling (HIBT) FETs for Low Voltage SRAMs" *IEEE Transactions on Electron Devices*, vol. 59, no.12, pp: 3533-3542, December 2012 (contributed equally by all authors)
- [54] Y. Zhu, N. Jain, S. Vijayaraghavan, D. K. Mohata\*, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, N. Monsegue, and M. K. Hudait "Defect assistant band alignment transition from staggered

to broken gap in mixed As/Sb tunnel field effect transistor heterostructure" *J. Appl. Phys.* 122, 094312 October 2012 (Fourth author supervised by the candidate)

[53] H. Madan\*, V. Saripalli\*, H. Liu\* , and S. Datta, "Asymmetric Tunnel Field-Effect Transistors as Frequency Multipliers" *IEEE Electron Device Letters* vol. 33, no. 11, pp. 1547-1549, November 2012 (First, second and third authors supervised by the candidate)

[52] D. K. Mohata\*, R. Bijesh\*, T. Mayer, J. Fastenau, D. Lubyshev, A. W. K. Liu, and S. Datta, "Barrier Engineered Arsenide-Antimonide Hetero-junction Tunnel FETs with Enhanced Drive Current" *IEEE Electron Device Letters* vol. 33, no. 11, pp. 1568-1570, November 2012 (First and second authors supervised by the candidate)

[51] J. D. Yearsley, J. C. Lin, E. Hwang\*, S. Datta, and S. E. Mohny "Ultra low-resistance palladium silicide Ohmic contacts to lightly doped n-InGaAs" *J. Appl. Phys.* 112, 054510, September 2012 (Third author supervised by the candidate)

[50] Y. Zhu, N. Jain, D. K. Mohata\*, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, and M. K. Hudait "Structural properties and band offset determination of p-channel mixed As/Sb type-II staggered gap tunnel field-effect transistor structure" *Appl. Phys. Lett.* 101, 112106 September 2012 (Third author supervised by the candidate)

[49] R. Bijesh\*, I. Ok, S. Mujumdar, C. Hobbs, P. Majhi, R. Janmmy, and S. Datta, "Correlated Flicker Noise and Hole Mobility Characteristics of (110)/<110> Uniaxially Strained SiGe FINFETs" *IEEE Electron Device Letters*, vol. 33, no. 09, pp. 1237-1239, September 2012. (First author supervised by the candidate)

[48] F. Li\*, R. Misra, Zhao Fang\*, Y. Wu, P. Schiffer, Q. M. Zhang, S. Tadigadapa and S. Datta, "Magnetolectric Flexural Gate Transistor with NanoTesla Sensitivity" *IEEE Journal of Microelectromechanical Systems (MEMS)*, vol 22, No 1, February 2013 (first and third authors supervised by the candidate)

[47] Y. Zhu, N. Jain, S. Vijayaraghavan, D. K. Mohata\*, S. Datta, D. Lubyshev, J. M. Fastenau, W. K. Liu, N. Monsegue, and M. K. Hudait, "Role of InAs and GaAs terminated heterointerfaces at source/channel on the mixed As-Sb staggered gap tunnel field effect transistor structures grown by molecular beam epitaxy" *Journal of Applied Physics*, 112, 024306 July 2012 (Fifth author supervised by the candidate).

[46] A. Agrawal\*, N. Shukla\*, K. Ahmed, and S. Datta, "A Unified Model for Insulator Selection to Form Ultra-Low Resistivity Metal-Insulator-Semiconductor Contacts to n-Si, n-Ge and n-

InGaAs" *Applied Physics Letters*,101, 042108, July 2012 (first and second authors supervised by candidate)

[45] L. Liu\*, D. K. Mohata\*, and S. Datta, "Scaling Length Theory of Double-Gate Interband Tunnel Field-Effect Transistors" *IEEE Transactions on Electron Devices*, 59(4), pp. 902-908, April 2012 (First and second authors supervised by candidate)

[44] W. Cho, M. Luisier, D. K. Mohata\*, S. Datta, D. Pawlik, S. L. Rommel, and G. Klimeck "Full band atomistic modeling of homo-junction InGaAs band-to-band tunneling diodes including band gap narrowing" *Applied Physics Letters*,100(6), pp. 063504 - 063504-3 ,February 2012 (Third author supervised by the candidate)

[43] S. Mujumdar\*, K. Maitra, and S. Datta "Layout dependent strain optimization for p-channel Non-planar Tri-gate Transistors" *IEEE Transactions on Electron Devices*, vol 59, no. 1, pp. 72-78, January 2012. (First author supervised by the candidate)

[42] A. Ali\*, H. Madan\*, A. Agrawal\*, I. Ramirez, R. Misra, J. B. Boos, B. R. Bennett, J. Lindemuth and S. Datta, "Enhancement Mode Antimonide Quantum Well MOSFETs with High Electron Mobility and GHz Small-Signal Switching Performance," *IEEE Electron Device Letters*, vol 32, no 12, 1689 – 1691, December 2011 (First, second and third authors supervised by the candidate)

[41] Matthew J Hollander\*, Michael LaBella, Zachary R Hughes, Michael Zhu, Kathleen A Trumbull, Randal Cavalero, David W Snyder, Xiaojun Wang, Euichul Hwang, Suman Datta, and Joshua A Robinson, "Enhanced Transport and Transistor Performance with Oxide Seeded High-k Gate Dielectrics on Wafer-Scale Epitaxial Graphene," *Nano Letters*, p. 110804163939013, Aug. 2011. (First author supervised by the candidate)

[40] Vinay Saripalli\*, Guangyu Sun, Asit Mishra, Yuan Xie, Suman Datta and Vijaykrishnan Narayanan, "Exploiting Heterogeneity for Energy Efficiency in Chip Multiprocessors," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, June 2011. (Invited paper) (First author supervised by the candidate)

[39] E.Hwang\*, S.Mookerjea\*, M.K Hudait, S.Datta, "Investigation of scalability of In<sub>0.7</sub>Ga<sub>0.3</sub>As quantum well field effect transistor (QWFET) architecture for logic applications," *Solid-State Electronics*, vol. 62, pp. 82-89, August 2011. (First and second authors supervised by the candidate)

[38] D. Mohata\*, S. Mookerjea\*, A. Agrawal\*, Y. Li, T. Mayer, V. Narayanan, A. Liu and S. Datta, "Experimental Staggered-Source and N<sup>+</sup> Pocket-Doped Channel III-V Tunnel Field-Effect



Transistors and Their Scalabilities," *Applied Physics Express*, vol 4, pp. 024105, February 2011 (First, second and third authors supervised by the candidate)

[37] A. Ali\*, B. Bennett, B. Boos, H. Madan\*, A. Agrawal\*, P. Schiffer, R. Misra and S. Datta, , "Experimental Determination of Quantum and Centroid Capacitance in Arsenide-Antimonide Quantum-Well MOSFETs Incorporating Non-Parabolicity Effect," *IEEE Transactions on Electron Devices* , vol. 58 , pp. 1397-1403, January 2011 (First and fourth authors supervised by the candidate)

[36] L. Liu\* and S. Datta, "A Generalized Scaling Length Theory for Double Gate Inter-band Tunnel FETs," accepted for publication in *IEEE Transactions on Electron Devices*, number of pages: 6, Dec 2011 (first author supervised by the candidate)

[35] A. Vallett, S. Minassian, P. Kaszuba, S. Datta, J. M. Redwing and T.S. Mayer, "Fabrication and Characterization of Axially Doped Silicon Nanowire Tunnel Field-Effect Transistors," *NanoLetters*, vol. 10, pp. 4813-4818, November 2010.

[34] I. Geppert, M. Eizenberg, A. Ali\* and S. Datta, "Band offsets determination and interfacial chemical properties of the Al<sub>2</sub>O<sub>3</sub>/GaSb system," *Applied Physics Letters*, vol. 97, pp. 162109, October 2010 (Third author supervised by the candidate)

[33] W.C. Kao\*, A. Ali, E. Hwang\*, S. Mookerjee\* and S. Datta "Effect of interface states on sub-threshold response of III-V MOSFETs, MOS HEMTs and tunnel FETs", *Solid-State Electronics*, vol.54, pp. 16665-1668, August 2010. (First, second, third and fourth authors supervised by the candidate)

[32] A. Ali\*, H. S. Madan\*, A. P. Kirk, R. M. Wallace, D. A. Zhao, D. A. Mourey, M. K. Hudait, T. N. Jackson, B. R. Bennett, J. B. Boos, and S. Datta, "Fermi Level Unpinning of GaSb (100) using Plasma Enhanced Atomic Layer Deposition of Al<sub>2</sub>O<sub>3</sub> Dielectric," submitted to *Applied Physics Letters*, number of pages: 3, July 2010 (First and second authors supervised by the candidate)

[31] V. Saripalli\*, L. Liu\*, S. Datta and V. Narayanan "Energy-Delay Analysis of Single Electron Transistor Based BDD Logic," *Journal of Low Power Electronics*, Vol, 6, No. 3, pp. , October 2010 (First and second authors supervised by the candidate)(This paper featured on the cover page of the journal)

- [30] F. Li\*, F. Zhao\*, Q. M. Zhang, and S. Datta, "Low Frequency Voltage Mode Sensing of Magnetoelectric Sensor in Package," *Electronics Letters*, Vol. 46, No. 16, pp. August 2010 (First and second authors supervised by the candidate)
- [29] S. Mookerjea\*, D. Mohata\*, T. Mayer, V. Narayanan, S. Datta, "Temperature-Dependent Characteristics of a Vertical In<sub>0.53</sub>Ga<sub>0.47</sub>As Tunnel FET," *IEEE Electron Device Letters*, Vol. 31, No. 6, pp. 564-567, June 2010. (First and second authors supervised by the candidate)
- [28] A. Ali\*, H. Madan\*, S. Koveshnikov, S. Oktyabrsky, R. Kambhampati, T. Heeg, D. Schlom, and S. Datta, "Small signal response of inversion layers in high mobility In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSFETs made with thin high-k dielectrics," *IEEE Transactions on Electron Devices*, Vol. 57, No. 4, p. 742-748, April 2010. (First and second authors supervised by the candidate)
- [27] B. Downey, S. Datta and S. Mohny, "Numerical study of reduced contact resistance via nanoscale topography at metal/semiconductor interfaces," *Semiconductor Science and Technology*, Vol. 25, No. 1, pp 1-4, January 2010. (Equal contributions by all authors)
- [26] F. Li\*, S. H. Lee, Z. Fang\*, P. Majhi, Q. Zhang, S. K. Banerjee, and S. Datta, "Flicker Noise Improvement in 100 nm Lg Si<sub>0.50</sub>Ge<sub>0.50</sub> Strained Quantum-Well Transistors using Ultra-Thin Si Cap Layer," *IEEE Electron Device Letters*, vol. 31, No. 1, pp. 47-49, January 2010. (First author supervised and third author co-supervised by the candidate)
- [25] S. Mookerjea\*, R. Krishnan\*, S. Datta, and V. Narayanan, "On Enhanced Miller Capacitance in Inter-Band Tunnel Transistors," *IEEE Electron Device Letters*, Vol. 30, No. 10, pp. 1102-1104, October 2009. (First author supervised and second author co-supervised by candidate)
- [24] A. Ali\*, H. Madan\*, S. Koveshnikov and S. Datta," Small Signal Response of Inversion Layers in High Mobility In<sub>0.53</sub>Ga<sub>0.47</sub>As MOSFETs Made with Thin High-k Dielectrics", *Electrochemical Society (ECS) Transactions*, Vol. 25, No. 6, pp. 271-284, Physics and Technology of High-k Gate Dielectrics, October 2009. (First and second authors supervised by the candidate)(Based on candidate's invited talk)
- [23] S. Mookerjea\*, R. Krishnan\*, S. Datta, and V. Narayanan, "Effective Capacitance and Drive Current for Tunnel-FET (TFET) CV/I Estimation," *IEEE Transactions on Electron Devices*, Vol. 56, No. 9, pp. 2092-2098, September 2009. (First author supervised and second author co-supervised by candidate)
- [22] Z. Fang\*, S. G. Lu, F. Li\*, S. Datta, and Q. M. Zhang, "Enhancing the Magnetoelectric Response of Metglas/Polyvinylidene fluoride Laminates by Exploiting the Flux Concentration

Effect,” *Applied Physics Letters*, Vol. 95, No. 11, pp. 112903\_1-112903\_3, September 2009. (First author co-supervised and third author supervised by the candidate)

[21] S. Mookerjee\*, R. Krishnan\*, A. Vallett, T. Mayer and S. Datta, “Inter-band Tunnel Transistor Architecture using Narrow Gap Semiconductors”, *ECS Transactions*, Vol 19, No. 5, Ge and III-V MOSFETs, pp. 287-292, May 2009. (First author co-supervised and third author supervised by the candidate) (Based on Invited Talk by the candidate)

[20] D. Schlom, S. Guha, and S. Datta, "Gate Oxides Beyond SiO<sub>2</sub>," *MRS Bulletin*, pp. 1017-1025, November 2008. (Equal contributions by all authors)

[19] S. H. Lee, P. Majhi, J. Oh, B. Sassman, C. Young, A. Bowonder, W. Y. Loh, J. J. Choi, B. J. Cho, H. D. Lee, P. Kirsch, H. R. Harris, W. Tsai, S. Datta, H. H. Tseng, S. K. Banerjee, and R. Jammy, "Demonstration of Lg 55 nm pMOSFETs With Si Si<sub>0.25</sub>Ge<sub>0.75</sub> Si Channels, High Ion Ioff ( $5 \times 10^4$ ), and Controlled Short Channel Effects (SCEs)," *IEEE Electron Device Letters*, Vol. 29, No 9, pp. 1017-1020, September 2008. (Equal contribution by all authors)

[18] C. I. Kuo; H. T. Hsu, E. Y Chang, C. Y. Chang; Y. Miyamoto, S. Datta; M. Radosavljevic, G-W. Huang, and C. T. Lee, “RF and Logic Performance Improvement of In<sub>0.7</sub>Ga<sub>0.3</sub>As}/InAs/In<sub>0.7</sub>Ga<sub>0.3</sub>As Composite-Channel HEMT Using Gate-Sinking Technology,” *IEEE Electron Device Letters*, Vol. 29, Issue 4, pp. 290-293, 2008. (Equal contribution by all authors)

[17] R. Chau, B. Doyle, S. Datta, K. Kavalieros, and K. Zhang, “Integrated nanoelectronics for the future,” *Nature Materials*, Vol. 6, pp. 810-812, 2007. (Equal contribution by all authors)

[16] S. Datta, G. Dewey, J. M. Fastenau, M. K. Hudait, D. Loubychev, W. K. Liu, M. Radosavljevic, W. Rachmady, and R. Chau, “Ultrahigh-Speed 0.5 V Supply Voltage In<sub>0.7</sub>Ga<sub>0.3</sub>As Quantum-Well Transistors on Silicon Substrate,” *IEEE Electron Device Letters*, Vol. 28, No. 8, pp. 685, 2007. (Nominated for the George E. Smith award for the best 2007 EDL paper by IEEE Electron Devices Society)

[15] S. Datta, “III-V field-effect transistors for low power digital logic applications,” *Journal of Microelectronic Engineering*, Vol. 84, No. 9-10, pp. 2133-2137, 2007. (Invited paper) (This paper is cited several times in the Emerging Research Devices section of the 2007 edition of the International Technology Roadmap for Semiconductors (ITRS). ITRS is a vital reference for the semiconductor industry and addresses the technology challenges and possible solutions for the industry over the next 15 years)

- [14] C. Y. Chang, H. T. Hsu, E. Y. Chang, C. I. Kuo, S. Datta, M. Radosavljevic, M. Miyamoto, and G. W. Y. Huang, "Investigation of Impact Ionization in InAs-Channel HEMT for High-Speed and Low-Power Applications," *IEEE Electron Device Letters*, Vol. 28, No. 10, pp. 856-858, 2007. (Equal contributions by all authors)
- [13] T. Ashley, L. Buckle, S. Datta, M.T. Emeny, D.G. Hayes, K.P. Hilton, R. Jefferies, T. Martin, T.J. Phillips, D.J. Wallis, P.J. Wilding, and R. Chau, "Heterogeneous InSb quantum well transistors on silicon for ultra-high speed, low power logic applications," *Electronics Letters*, Vol. 43, No. 14, 2007. (Equal contribution by all authors)
- [12] R. Chau, S. Datta, M. Doczy, B. S. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M. Radosavljevic, "Benchmarking nanotechnology for high-performance and low-power logic transistor applications," *IEEE Transactions on Nanotechnology*, Vol. 4, No. 2, pp. 153-158, 2005. (Equal contribution by all authors)
- [11] R. Chau, J. Brask, S. Datta, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, B. Jin, M. Metz, A. Majumdar, and M. Radosavljevic, "Application of high-K gate dielectrics and metal gate electrodes to enable silicon and non-silicon logic nanotechnology," *Journal of MicroElectronic Engineering*, Vol. 80, No. 17, pp. 1-6, 2005. (Equal contribution by all authors)
- [10] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-K/Metal-Gate Stack and its MOSFET Characteristics," *IEEE Electron Device Letters*, Vol. 25, No. 6, pp. 408-410, 2004. (Equal contribution by all authors)
- [9] R. Chau, B. Boyanov, B. Doyle, M. Doczy, S. Datta, S. Hareland, B. Jin, J. Kavalieros, and M. Metz, "Silicon Nano-transistors for Logic Applications," *Physica E, Low-Dimensional Systems and Nanostructures*, Vol. 19, No. 1-2, pp. 1-5, 2003. (Equal contribution by all authors)
- [8] B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, and R. Chau, "High Performance Fully-Depleted Tri-Gate CMOS Transistors," *IEEE Electron Device Letters*, Vol. 24, No. 4, pp. 263-265, 2003. (Equal contribution by all authors)
- [7] S. Datta, K. P. Roenker, M. M. Cahay, and L. M. Lunardi, "Analytical Modeling of Pnp InP/InGaAs Heterojunction Bipolar Transistors," *Solid-State Electronics*, Vol. 44, No. 7, pp. 1331-1333, 2000.
- [6] S. Datta, K. P. Roenker, and M. M. Cahay, "A Gummel-Poon Model for Pnp Heterojunction Bipolar Transistors with a Compositionally Graded Base," *Solid-State Electronics*, Vol. 44, No. 6, pp. 991-1000, 2000.

- [5] S. Datta, K. P. Roenker, and M. M. Cahay, "Emitter Series Resistance Effect of Multiple Heterojunction Contacts for Pnp Heterojunction Bipolar Transistors," *Solid-State Electronics*, Vol. 43, No. 7, pp. 1299-1305, 1999.
- [4] S. Datta, K. P. Roenker, and M. M. Cahay, "Hole Transport and Quasi-Fermi Level Splitting at the Emitter-Base Junction in Pnp Heterojunction Bipolar Transistors," *Journal of Applied Physics*, Vol. 85, No. 3, pp. 1949-1955, 1999.
- [3] S. Datta, K. P. Roenker, and M. M. Cahay, "Implications of Hole versus Electron Transport Properties for High Speed Pnp Heterojunction Bipolar Transistors," *Solid-State Electronics*, Vol. 43, No. 1, pp. 73-80, 1999.
- [2] S. Datta, S. Shi, K. P. Roenker, and M. M. Cahay and W. E. Stanchina, "Simulation and Design of InAlAs/InGaAs Pnp Heterojunction Bipolar Transistors," *IEEE Transactions on Electron Devices*, Vol. 45, No. 8, pp. 1634-1643, 1998.
- [1] S. Datta, K. P. Roenker, and M. M. Cahay, "A Thermionic-Emission-Diffusion Model for a Graded Base Pnp Heterojunction Bipolar Transistors," *Journal of Applied Physics*, Vol. 83, No. 12, pp. 8036-8045, 1998

#### **Refereed Conference Proceedings Articles**

- [109] A. Aziz, N. Shukla, S. Datta and S. K Gupta, "Implication of Hysteretic Selector Device on the Biasing Scheme of a Cross-point Memory Array", International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 2015, Washington DC, USA.
- [108] Ram Krishna Ghosh, Yu-Chuan Lin, Joshua A. Robinson and Suman Datta "Heterojunction resonant tunneling diode at the atomic limit", International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 2015, Washington DC, USA
- [107] A. Aziz, N. Shukla, S. Datta and S. K Gupta, "COAST: Correlated Material Assisted STT MRAMs for Optimized Read Operation", International Symposium on Low Power Electronics and Design (ISLPED), 2015, Rome, Italy
- [106] M. Barth, H. Liu, J. H. Warner, B. R. Bennett, D. McMorro, N. Roche, P. Paillet, M. Gaillardin, and S. Datta "Single Event Measurement and Analysis of Antimony based n-channel Quantum-Well MOSFET with High-k Dielectric" 2015 NSREC Boston MA, July 2015
- [105] M. Barth, G. Bruce Rayner, R. Engel-Herbert, and S. Datta "Preparation of high quality high-k/GaSb interfaces using in-situ spectroscopic ellipsometry and reflection high energy electron diffraction" 2015 AVS ALD Conference, Portland OR June 2015

- [104] R. Pandey, H. Madan, H. Liu, V. Chobpattana, M. Barth, B. Rajamohanam, M. J. Hollander, T. Clark, K. Wang, J.-H. Kim, D. Gundlach, K. P. Cheung, J. Suehle, R. Engel-Herbert, S. Stemmer and S. Datta, "Demonstration of p-type In<sub>0.7</sub>Ga<sub>0.3</sub>As/GaAs<sub>0.35</sub>Sb<sub>0.65</sub> and n-type GaAs<sub>0.4</sub>Sb<sub>0.6</sub>/In<sub>0.65</sub>Ga<sub>0.35</sub>As Complimentary Heterojunction Vertical Tunnel FETs for Ultra-Low Power Logic", IEEE Symposia on VLSI Technology and Circuits, Kyoto, 2015.
- [103] A. V. Thathachary, N. Agrawal, K. K. Bhuiwala, M. Cantoro, Y-C Heo, G. Lavalley, S. Maeda, and S. Datta, "Indium Arsenide (InAs) Single and Dual Quantum-Well Heterostructure FinFETs", IEEE Symposia on VLSI Technology and Circuits, Kyoto, 2015.
- [102] A. Aziz, N. Shukla, S. Datta and S. K. Gupta, "Read Optimized MRAM with Separate Read-Write Paths based on Concerted Operation of Magnetic Tunnel Junction with Correlated Material", Device Research Conference (DRC), Ohio State University, 2015.
- [101] R. Pandey, N. Agrawal, R. Arghavani, and S. Datta, "Analysis of Local Interconnect Resistance at Scaled Process Nodes", Device Research Conference (DRC), Ohio State University, 2015.
- [100] N. Agrawal, A. Agrawal, S. Mukhopadhyay, S. Mahapatra, and S. Datta, "Electron Trapping Dominance in Strained Germanium Quantum Well Planar and FinFET devices with NBTI", Device Research Conference (DRC), Ohio State University, 2015
- [99] A. Agrawal\*, M. Barth\*, G. B. Rayner Jr., Arun V. T.\*, C. Eichfeld, G. Lavalley, S-Y. Yu, X. Sang, S. Brookes, Y. Zheng, Y-J. Lee, Y-R. Lin, C-H. Wu, C-H. Ko, J. LeBeau, R. Engel-Herbert<sup>1</sup>, S. E. Mohny, Y-C. Yeo and S. Datta "Enhancement Mode Strained (1.3%) Germanium Quantum Well FinFET (W<sub>Fin</sub>=20nm) with High Mobility (Hole=700 cm<sup>2</sup>/Vs), Low EOT (~0.7nm) on Bulk Silicon Substrate", *IEEE International Electron Device Meeting (IEDM) Technical Digest*, pp. 414-417, December 2014 (First, second and fourth authors supervised by the candidate)
- [98] N. Shukla\*, A. Parihar, M. Cotter\*, M. Barth\*, X. Li, N. Chandramoorthy, H. Paik, D. G. Schlom, V. Narayanan, A. Raychowdhury and S. Datta, "Pairwise Coupled Hybrid Vanadium Dioxide-MOSFET (HVFET) Oscillators for Non-Boolean Associative Computing", *IEEE International Electron Device Meeting (IEDM) Technical Digest*, pp. 673-676, December 2014 (First, third and fourth authors supervised by the candidate)
- [97] Moon Seok Kim, Huichu Liu\*, Karthik Swaminathan, Xueqing Li, Suman Datta, Vijaykrishnan Narayanan "Enabling power-efficient designs with III-V Tunnel FETs" *IEEE*

*Compound Semiconductor IC Symposium (CSICS)*, October, 2014 (Second author supervised by the candidate)

[96] Matthew J. Hollander\*, Himanshu Madan\*, Gregory Pastir, Randal Cavalero, David Snyder, Joshua A. Robinson, and Suman Datta. "Enhanced Short-channel Performance and p-n Symmetry in Graphene Based Ambipolar Mixer Using Nano-ribbon Geometry" *4th International Symposium on Graphene Devices*, Sept. 2014 (First and second authors supervised by the candidate)

[95] Huichu Liu\*; Mahsa Shoaran; Xueqing Li; Suman Datta; Alexandre Schmid; Vijaykrishnan Narayanan, "Tunnel FET-Based Ultra-Low Power, Low-Noise Amplifier Design for Bio-signal Acquisition", *International Symposium on Low Power Electronics and Design (ISLPED)*, La Jolla, August 11-13, 2014 (First author supervised by the candidate)

[94] S. Datta, R. Pandey\*, S. Gupta, R. Arghavani, "Impact of Contact and Local Interconnect Scaling on Logic Performance", *IEEE Symposia on VLSI Technology and Circuits (VLSI)*, June 2014 (Second author supervised by the candidate) (invited talk)

[93] Arun. V Thathachary\*, N. Agrawal\*, G. Lavallee, M. Cantoro, S.-S. Kim, D.-W. Kim and S. Datta, "Investigation of In<sub>x</sub>Ga<sub>1-x</sub>As FinFET architecture with varying Indium (x) concentration and quantum confinement", *IEEE Symposia on VLSI Technology and Circuits (VLSI)*, June 2014 (First and second authors supervised by the candidate)

[92] S. Datta, N. Shukla\*, M. Cotter, A. Parihar, A. Raychowdhury, "Neuro Inspired Computing with Coupled Relaxation Oscillators", *ACM/EDAC/IEEE Annual Design Automation Conference (DAC)*, pp. 1-6, June 2014 (Second author supervised by the candidate) (invited talk)

[91] Vijaykrishnan Narayanan, Suman Datta, Gert Cauwenberghs, Don Chiarulli, Steve Levitan, and Philip Wong, "Video Analytics Using Beyond CMOS Devices", *Design, Automation and Test in Europe Conference and Exhibition (DATE)*, March 2014 (equal contribution by all authors) (invited talk)

[90] Chian-We Liu, Chang-En Chiang, Ching-Yi Huang, Chun-Yao Wang, Yung-Chih Chen, Suman Datta, Vijaykrishnan Narayanan, "Width Minimization in the Single-Electron Transistor Array Synthesis", *Design, Automation and Test in Europe Conference and Exhibition (DATE)*, 2014 March 2014 (equal contribution by all authors)

[89] R. Bijesh\*, H. Liu\*, H. Madan\*, D. Mohata\*, W. Li, N. V. Nguyen, D. Gundlach, C.A. Richter, J. Maier, K. Wang, T. Clarke, J. M. Fastenau, D. Loubychev, W. K. Liu, V. Narayanan and S. Datta, "Demonstration of InGaAs/GaAsSb Near Broken-gap Tunnel FET with

Ion=740uA/um, Gm=700uS/um and Gigahertz Switching Performance at VDS=0.5V", *IEEE International Electron Device Meeting (IEDM) Technical Digest*, pp. 687-690, December 2013 (First, second, third and fourth authors supervised by the candidate)

[88] H. Liu\*, S. Datta, and V. Narayanan "Steep Switching Tunnel FET: A Promise to Extend the Energy Efficient Roadmap for Post-CMOS Digital and Analog/RF Application" *International Symposium on Low Power Electronics and Design (ISLPED)* Beijing, China, September 4-6, 2013 (First author supervised by the candidate)

[87] H. Liu\*, R. Vaddi, S. Datta, and V. Narayanan "Tunnel FET based Ultra-Low Power, High Sensitivity UHF RFID Rectifier" *International Symposium on Low Power Electronics and Design (ISLPED)* Beijing, China, September 4-6, 2013 (First author supervised by the candidate)

[86] M. Barth\*, A. Agrawal\*, A. Ali\*, J. Fastenau, D. Loubychev, W.K. Liu and S. Datta "Compressively Strained InSb MOSFETs with High Hole Mobility for P-Channel Application" *IEEE Device Research Conference (DRC)*, University of Notre Dame, June 23-26, 2013 (First, second and third authors supervised by the candidate)

[85] Arun V. Thathachary\*, L. Liu\* and S.Datta "Impact of fin width scaling on carrier transport in III-V FinFETs" *IEEE Device Research Conference (DRC)*, University of Notre Dame, June 23-26, 2013. (First and second authors supervised by the candidate)

[84] Matthew J. Hollander\*, Nikhil Shukla\*, Nidhi Agrawal\*, Himanshu Madan\*, Joshua A. Robinson and Suman Datta "Reduction of Charge Transfer Region Using Graphene Nano-ribbon Geometry for Improved Complementary FET Performance at Sub-Micron Channel Length" *IEEE Device Research Conference (DRC)*, University of Notre Dame, June 23-26, 2013 (First, second, third and fourth authors supervised by the candidate)

[83] H. Madan\*, M. J. Hollander\*, J. A. Robinson, and S. Datta "Analysis and Benchmarking of Graphene Based RF Low Noise Amplifiers" *IEEE Device Research Conference (DRC)*, University of Notre Dame, June 23-26, 2013 (First and second authors supervised by the candidate).

[82] A. Agrawal\*, J. Lin, B. Zheng, S. Sharma, S. Chopra, K. Wang, A. Gelatos, S. Mohnchand, S. Datta "Barrier Height Reduction to 0.15eV and Contact Resistivity Reduction to  $9.1 \times 10^{-9} \Omega \text{ cm}^2$  Using Ultrathin TiO<sub>2-x</sub> Interlayer between Metal and Silicon" *IEEE Symposia on VLSI Technology and Circuits (VLSI)*, Kyoto, Japan, June 11-14, 2013. (First author supervised by the candidate)(nominated for best paper award)



- [81] H. Madan\*, M. J. Hollander\*, J. A. Robinson and S. Datta "Graphene Transistors for Ambipolar Mixing at Microwave Frequencies" *223rd Electrochemical Society Meeting*, Toronto, Ontario, Canada May 14-18 2013 (First and second authors supervised by the candidate)
- [80] S. Datta, R. Bijesh\*, H. Liu\*, D. Mohata\*, and V. Narayanan "Tunnel Transistors for Energy Efficient Computing" *IEEE International Reliability Physics Symposium (IRPS)*, Monterey, California, April 14- 18 2013 (Second, third and fourth authors supervised by the candidate) (invited paper)
- [79] K. Joshi, S. Hung, S. Mukhopadhyay, V. Chaudhary, N. Nanaware, B. Rajamohanan\*, T. Sato, M. Bevan, A. Wei, A. Noori, B. Mc.Dougal, C. Ni, G. Saheli, C. Lazik, P. Liu, D. Chu, L. Date, S. Datta, A. Brand, J Swenberg, and S. Mahapatra "HKMG Process Impact on N, P BTI: Role of Thermal IL Scaling, IL/HK Integration and Post HK Nitridation" *IEEE International Reliability Physics Symposium (IRPS)*, Monterey, California, April 14- 18 2013 (Sixth author supervised by the candidate)
- [78] H. Madan\*, M.J. Hollander\*, M. LaBella, R. Cavalero, D. Snyder, J. A. Robinson and S. Datta, "Record High Conversion Gain Ambipolar Graphene Mixer at 10 GHz Using Scaled Gate Oxide", *IEEE International Electron Device Meeting (IEDM) Technical Digest*, pp. 76-79, December 2012 (First and second authors supervised by the candidate)
- [77] Huichu Liu\*, Matthew Cotter, Suman Datta and Vijay Narayanan, "Technology Assessment of Si and III-V FinFETs and III-V Tunnel FETs from Soft Error Rate Perspective", *IEEE International Electron Device Meeting (IEDM) Technical Digest*, pp. 577-580, December (2012) (First author supervised by the candidate)
- [76] E. Kultursay , K. Swaminathan , V. Saripalli\*, S. Datta , V. Narayanan, and M. Kandemir, "Performance Enhancement under Power Constraints using Heterogeneous CMOS-TFET Multicores" *IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis*, Oct 7-12, 2012 (Third author supervised by the candidate)
- [75] R. Mukundrajana\*, M. Cotter, V. Saripalli\*, M. J. Irwin, S. Datta, and V. Narayanan, "Ultra Low Power Circuit Design using Tunnel FETs" *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Aug 19-21, Amherst, USA (First and third authors supervised by the candidate)
- [74] M. J. Hollander\*, A. Agrawal\*, M. S. Bresnehan, M. LaBella, K. A. Trumbull, R. Cavalero, S. Datta, and Joshua A. Robinson, "High Performance, Large Area Graphene Transistors on Quasi-Free-Standing Graphene Using Synthetic Hexagonal Boron Nitride Gate Dielectrics" *IEEE Device*

*Research Conference (DRC)*, Penn State University, June 18-20, 2012 (First and second authors supervised by the candidate) (won best paper award)

[73] M. J. Hollander\*, A. Agrawal\*, M. S. Bresnehan, M. LaBella, K. A. Trumbull, R. Cavalero, S. Datta, and Joshua A. Robinson, "Effect of Transferred Hexagonal Boron Nitride Dielectrics on Quasi-Freestanding Epitaxial Graphene" *Electronic Materials Conference (EMC)*, Penn State University, June 18-20, 2012 (First and second authors supervised by the candidate)

[72] H. Liu\*, D. K. Mohata\*, A. Nidhi\*, V. Saripalli\*, V. Narayanan and S. Datta, "Exploration of Vertical MOSFET and Tunnel FET Device Architecture for Sub 10nm Node Applications" *IEEE Device Research Conference (DRC)*, Penn State University, June 18-20, 2012 (first, second, third and fourth authors supervised by the candidate).

[71] H. Madan\*, M. J. Hollander\*, J. A. Robinson, and S. Datta, "Extraction of Near Interface Trap Density in Top Gated Graphene Transistor Using High Frequency Current Voltage Characteristics" *IEEE Device Research Conference (DRC)*, Penn State University, June 18-20, 2012 (First and second authors supervised by the candidate)

[70] A. Agrawal\*, J. Park, D. K. Mohata\*, K. Ahmed, and S. Datta, "Experimental Demonstration of "Cold" Low Contact Resistivity Ohmic Contacts on Moderately Doped n-Ge with in-situ Atomic Hydrogen Clean" *IEEE Device Research Conference (DRC)*, Penn State University, June 18-20, 2012 (First and third authors supervised by the candidate).

[69] E. Freeman\*, A. Kar\*, N. Shukla\*, R. Misra, R. Engel-Herbert, D. Schlom, V. Gopalan, K. Rabe, and S.Datta, "Characterization and Modeling of Metal-Insulator Transition (MIT) Based Tunnel Junctions" *IEEE Device Research Conference (DRC)*, Penn State University, June 18-20, 2012 (First, second and third authors supervised by the candidate)

[68] N. Agrawal\*, V.Saripalli\*, V.Narayanan, Y.Kimura, R.Arghavani, and S.Datta, "Will Strong Quantum Confinement Effect Limit Low Vcc Applications of III-V FinFETs?" *IEEE Device Research Conference (DRC)*, Penn State University, June 18-20, 2012 (First and second authors supervised by the candidate)

[67] R. Bijesh\*, D. K. Mohata\*, H. Liu\*, and S. Datta, "Flicker Noise Characterization and Analytical Modeling of Homo and Hetero-Junction III-V Tunnel FETs" *IEEE Device Research Conference (DRC)*, Penn State University, June 18-20, 2012 (First, second and third authors supervised by the candidate)

- [66] A. Ali\*, H. Madan\*, M. J. Barth\*, M. J. Hollander, J. B. Boos, B. R. Bennett, and S. Datta, "Antimonide NMOSFET with Source Side Injection Velocity of  $2.7 \times 10^7$  cm/s for Low Power High Performance Logic Applications" *IEEE Symposia on VLSI Technology and Circuits (VLSI)*, Honolulu, June 12-15, 2012 (First, second and third authors supervised by the candidate).
- [65] D. K. Mohata\*, R. Bijesh\*, Y. Zhu, M. K. Hudait, R. Southwick, Z. Chbili, D. Gundlach, J. Suehle, J. M. Fastenau, D. Loubychev, A. K. Liu, T. S. Mayer, V. Narayanan and S. Datta, "Demonstration of Improved Heteroepitaxy, Scaled Gate Stack and Reduced Interface States Enabling Heterojunction Tunnel FETs with High Drive Current and High On-Off Ratio" *IEEE Symposia on VLSI Technology and Circuits (VLSI)*, Honolulu, June 12-15, 2012 (First and second authors supervised by the candidate)
- [64] K. Ahmed, S. Chopra, A. Agrawal\* and S. Datta "Benchmarking of Novel Contact Architectures on Silicon and Germanium" *International Silicon-Germanium Technology and Device Meeting (ISTDM)*, June 4-6 2012 (Third author supervised by the candidate)
- [63] F. Li\*, R. Misra, Z. Fang, C. Curwen, Y. Wu, Q. M. Zhang, P. Schiffer, S. Tadigadapa, and S. Datta, "Magnetolectric Resonant Gate Transistor" *Solid-State Sensors, Actuators, and Microsystems Workshop*, Hilton Head, June 3-7, 2012 (First author supervised by the candidate)
- [62] K. Ahmed, A. Agrawal\*, S. Chopra, and S. Datta, "Benchmarking of Novel Contact Architectures on Silicon and Germanium" *International Silicon-Germanium Technology and Device Meeting (ISTDM)*, June 4, 2012
- [61] D. K. Mohata, R. Bijesh, S. Mujumdar, C. Eaton, R. Engel-Herbert, T. Mayer, V. Narayanan, J. Fastenau, D. Loubychev, A. Liu and S. Datta, "Demonstration of MOSFET-Like On-Current Performance in Arsenide/Antimonide Tunnel FETs with Staggered Hetero-junctions for 300mV Logic Applications", *IEEE International Electron Devices Meeting Technical Digest*, pp. 33.5.1 - 33.5.4, Dec. 5-7, 2011 (First, second and third authors supervised by the candidate)
- [60] L. Liu\*, V. Saripalli\*, V. Narayanan and S. Datta, "Device Circuit Co-Design Using Classical and Non-Classical III-V Multi-Gate Quantum-Well FETs (MuQFETs)", *IEEE International Electron Devices Meeting Technical Digest*, 4.5.1 - 4.5.4, Dec. 5-7, 2011 (First and second authors supervised by the candidate)
- [59] V. Saripalli\*, J. P. Kulkarni, N. Vijaykrishnan and S. Datta, "Variation-Tolerant Ultra Low-Power Heterojunction Tunnel FET SRAM Design", *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, pp. 45 – 52, July 2011 (First author supervised by the candidate)

- [58] A. Agrawal\*, A. Ali\*, R. Misra, P. E. Schiffer, J. B. Boos, B. R. Bennett and S. Datta, "Low Field Electron Transport in Mixed Arsenide Antimonide Quantum Well Heterostructures", Electronic Materials Conference (EMC), Univ. of California, Santa Barbara, June 2011 (First and second authors supervised by the candidate)
- [57] A. Agrawal\*, A. Ali\*, R. Misra, P. E. Schiffer, B. R. Bennett, J. B. Boos and S. Datta, "Experimental Determination of Dominant Scattering Mechanisms in Scaled InAsSb Quantum Well", Device Research Conference (DRC), Univ. of California, Santa Barbara, pp. 27-28, June 2011 (First and second authors supervised by the candidate)
- [56] R. Bijesh\*, I. OK, M. Baykan, C. Hobbs, P. Majhi, R. Jammy and S. Datta, "Hole Mobility Enhancement in Uniaxially Strained SiGe FINFETs: Analysis and Prospects", Device Research Conference (DRC), Univ. of California, Santa Barbara, pp. 237-238, June 2011 (First author supervised by the candidate)
- [55] D. K. Mohata\*, R. Bijesh\*, V. Saripalli\*, T. Mayer and S. Datta, "Self-aligned Gate NanoPillar In<sub>0.53</sub>Ga<sub>0.47</sub>As Vertical Tunnel Transistor", Device Research Conference (DRC), Univ. of California, Santa Barbara, pp. 203-204, June 2011 (First, second and third authors supervised by the candidate)
- [54] F. Li\*, Z. Fang\*, R. Misra, S. Tadigadapa, Q. Zhang and S. Datta, "Giant magnetoelectric effect in nanofabricated Pb(Zr<sub>0.52</sub>Ti<sub>0.48</sub>)O<sub>3</sub>-Fe<sub>85</sub>B<sub>5</sub>Si<sub>10</sub> Cantilevers and resonant gate transistors", Device Research Conference (DRC), Univ. of California, Santa Barbara, pp. 237-238, pp. 69-70, June 2011 (First and second authors supervised by the candidate)
- [53] L. Liu\*, V. Saripalli\*, V. Narayanan and S. Datta, "Experimental Investigation of Scalability and Transport in In<sub>0.7</sub>Ga<sub>0.3</sub>As Multi-Gate Quantum Well FET (MuQFET)", Device Research Conference (DRC), Univ. of California, Santa Barbara, pp. 17-18, June 2011 (First and second authors supervised by the candidate)
- [52] H. Madan\*, D. Veksler, Y.T. Chen, J. Huang, N. Goel, G. Bersuker and S. Datta, "Interface States at high-k/InGaAs interface: H<sub>2</sub>O vs. O<sub>3</sub> based ALD Dielectric", Device Research Conference (DRC), Univ. of California, Santa Barbara, pp. 117-118, June 2011 (First author supervised by the candidate)
- [51] C. D. Young, M. Baykan, A. Agrawal\*, H. Madan\*, K. Akarvardar, C. Hobbs, I. OK, W. Taylor, C. E. Smith, M. M. Hussain, T. Nishida, S. Thompson, P. Majhi, P. Kirsch, S. Datta and R. Jammy, "Critical Discussion on (100) and (110) Orientation Dependent Transport : nMOS Planar

and FinFET", Intl. Symposium on VLSI Technology (VLSI), Kyoto, Japan, June, 2011. (Third and fourth authors supervised by the candidate)

[50] L. Liu\*, V. Saripalli\*, E. Hwang\*, V. Narayanan and S. Datta, "Multi-Gate Modulation Doped In<sub>0.7</sub>Ga<sub>0.3</sub>As Quantum Well FET for Ultra Low Power Digital Logic", accepted for publication in 219th Electro chemical Society (ECS) Meeting, Montreal, Canada, May 1-6, 2011. (First, second and third authors supervised by the candidate)

[49] V. Saripalli\*, A. Misra, S. Datta and V. Narayanan, "An Energy-Efficient Heterogeneous CMP based on Hybrid TFET-CMOS Cores," Design Automation Conference (DAC), San Diego, June 5-10, 2011. (First author supervised by the candidate)

[48] Y.C. Chen, S. Soumya, G. Sun, Y. Xie, S. Datta and V. Narayanan, "Automated Mapping for Reconfigurable Single Electron Transistor Arrays," Design Automation Conference (DAC) , San Diego, June 5-10, 2011

[47] Z. Fang\*, F. Li\*, N. Mokhariwale, S. Datta, and Q. M. Zhang, "Direct integration of magnetoelectric sensors with microelectronics—Improved field sensitivity, signal-to-noise ratio and frequency response," pp.15-16, *IEEE Sensors 2010 Conference*, pp. 614–619, Waikoloa, Hawaii, November 2010 (First and second authors supervised by the candidate)

[46] A. Ali, H. Madan, R. Misra, E.Hwang, A. Agrawal, P. Schiffer, J. B. Boos, B. R. Bennett, I. Geppert, M. Eizenberg and S. Datta, "Advanced Composite High-κ Gate Stack for Mixed Anion Arsenide-Antimonide Quantum Well Transistors" *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, December 2010 (First author supervised by the candidate)

[45] S. Datta "Compound Semiconductor Based Tunnel Transistor Logic," *Lester Eastman Conference on High Performance Devices (LEC)*, pp.178-179, Troy, USA, August 2010. (Invited talk by the candidate)

[44] S. Datta, A. Ali, S. Mookerjea, V. Saripalli, L. Liu, S. Eachempati, T. Mayer and V. Narayanan, "Non-silicon logic elements on silicon for extreme voltage scaling," *Proceedings of the Silicon Nanoelectronics Workshop (SNW)*, pp.15-16, Honolulu, Hawaii, June 2010. (Invited talk by the candidate)

[43] A.Ali\*, H. S. Madan\*, A. P. Kirk, R.M. Wallace, D. A. Zhao, D. A. Mourey, M. Hudait, T. N. Jackson, B. R. Bennett, J. B. Boos, and S. Datta, "Fermi Level Unpinning of GaSb(100) using Plasma Enhanced ALD Al<sub>2</sub>O<sub>3</sub> Dielectric," *IEEE Device Research Conference Digest*, pp. 27-28, South Bend, Indiana, June 2010. (First and second authors supervised by the candidate)

- [42] E. Hwang\*, S. Mookerjea\*, M. Hudait and S. Datta, "Scalability Study of In<sub>0.70</sub>Ga<sub>0.30</sub>As HEMTs for 22nm node and beyond Logic Applications," *IEEE Device Research Conference Digest*, pp. 61-62, South Bend, Indiana, June 2010. (First and second authors supervised by the candidate)
- [41] A.Vallett, S. Minassian, S. Datta, J. Redwing and T. Mayer,"Fabrication of Axially-Doped Silicon Nanowire Tunnel FETs and Characterization of Tunneling Current," *IEEE Device Research Conference Digest (DRC)*, pp. 273-274, South Bend, Indiana, June 2010. (Equal contribution by all authors)
- [40] D. Pawlik, M. Barth, P. Thomas, S. Kurinec, S. Mookerjea\*, D. Mohata\*, S. Datta, S. Cohen, D. Ritter, S. Rommel, "Sub-Micron In<sub>0.53</sub>Ga<sub>0.47</sub>As Esaki Diodes With Record Current Density of 1MA/cm<sup>2</sup>," *IEEE Device Research Conference Digest (DRC)*, pp. 163-164, South Bend, Indiana, June 2010. (Fifth and sixth authors supervised by the candidate)
- [39] D. K. Mohata\*, D. Pawlik, L. Liu\*, S. Mookerjea\*, V. Saripalli\*, S. Rommel and S. Datta,"Implications of Record Peak Current Density In<sub>0.53</sub>Ga<sub>0.47</sub>As Esaki Tunnel Diode on Tunnel FET Logic Applications," *IEEE Device Research Conference Digest (DRC)*, pp. 101-102, South Bend, Indiana, June 2010. (First, third, fourth, and fifth authors supervised by the candidate)
- [38] L. Liu\* and S. Datta,"Investigation of the Scalability of Ultra Thin Body Double Gate Tunnel FET using Physics based 2D Analytical Model," *IEEE Device Research Conference Digest (DRC)*, pp. 15-16, South Bend, Indiana, June 2010. (First author supervised by the candidate)
- [37] V. Saripalli\*, D. K. Mohata\*, S. Mookerjea\*, S. Datta and V. Narayanan,"Low Power Loadless 4T SRAM cell based on Degenerately Doped Source (DDS) In<sub>0.53</sub>Ga<sub>0.47</sub>As Tunnel FETs," *IEEE Device Research Conference Digest (DRC)*, pp. 103-104, South Bend, Indiana, June 2010. (First author supervised and second, third authors supervised by the candidate)
- [36] S. Datta, S. Mookerjea, D. Mohata, L. Liu, V. Saripalli, V. Narayanan and T. Mayer "Compound Semiconductor Based Tunnel Transistor Logic," *IEEE CS MANTECH Conference*, pp. 203-204, Portland, Oregon, May 2010 (Invited talk by the candidate)
- [32] S. Datta, "III-V compound MOSFET and TFET devices," *Proceedings of the IEEE 11th Ultimate Integration of Silicon (ULIS) Conference*, Glasgow, Scotland, March 2010. (Plenary Invited Talk by the candidate)
- [35] J. Singh\*, R. Krishnan\*, S. Mookerjea\*, S. Datta, V. Narayanan,"A Novel Si TFET Based SRAM design for Ultra Low-Power 0.3V VDD Applications," *Proceedings of 15th Asia South*

*Pacific Design Automation Conference (ASPDAC)*, Yokohama, Japan, January 2010. (First and second author co-supervised and third author supervised by the candidate)

[34] V. Saripalli\*, S. Datta and V. Narayanan "Analyzing Energy-Delay Behavior in Room Temperature Single Electron Transistors," *23rd International Conference on VLSI Design*, pp. 399-404, Bangalore, India, January 2010. (First author co-supervised by the candidate)

[33] S. Mookerjea\*, D. Mohata\*, R. Krishnan\*, J. Singh\*, A. Vallett, A. Ali\*, T. Mayer, V. Narayanan, D. Schlom, A. Liu and S. Datta, "Experimental Demonstration of 100nm Channel Length In<sub>0.53</sub>Ga<sub>0.47</sub>As-based Vertical Inter-band Tunnel Field Effect Transistors (TFETs) for Ultra Low-Power Logic and SRAM Applications," *IEEE International Electron Devices Meeting (IEDM) Technical Digest*, pp. 949-951, Baltimore, Maryland, December 2009. (First, second and sixth authors supervised, third and fourth authors co-supervised by the candidate) (This paper received worldwide press coverage by leading semiconductor news agencies)

[32] Z. Fang\*, S. Lu, F. Li\*, N. Mokhariwale, S. Datta, and Q.M. Zhang, "Sensitivity enhancement of magnetic sensors based on Metglas/PVDF laminates using the flux concentration effect," *Nanoelectronic Devices for Defense and Security Conference (NANO DDS)*, Colorado Springs, Colorado, September 2009. (First author co-supervised and third author supervised by the candidate)

[31] S. Mookerjea\* and S. Datta, "Band-gap Engineered Hot Carrier Tunnel Transistors," *67th IEEE Device Research Conference (DRC)*, pp. 121-122, University Park, Pennsylvania, June 2009. (First author supervised by the candidate)

[30] A. Ali\*, S. Mookerjea\*, E. Hwang\*, S. Kovesnikov, S. Oktyabrsky, V. Tokranov, M. Yakimov, R. Kambhampati, W. Tsai, and S. Datta, "HfO<sub>2</sub> Gated, Self Aligned and Directly Contacted Indium Arsenide Quantum-well Transistors for Logic Applications – A Temperature and Bias Dependent Study," *67th IEEE Device Research Conference (DRC)*, pp. 55-56, University Park, Pennsylvania, June 2009. (First, second, and third authors supervised by the candidate)

[29] D. J. Pawlik, P. Thomas, M. Barth, K. Johnson, S.L. Rommel, S. Mookerjea\*, S. Datta, M. Luisier, G. Klimeck, Z.Cheng, J. Li, J.S. Park, J.M. Hydrick, J.G. Fiorenza, and A. Lochtefeld, "Indium Gallium Arsenide on Silicon Interband Tunnel Diodes for NDR-based memory and Steep Subthreshold Slope Transistor Applications," *67th IEEE Device Research Conference (DRC)*, pp. 69-70, University Park, Pennsylvania, June 2009. (Sixth author supervised by the candidate)

- [28] N. Goel, D. Heh, S. Kovesnikov, I. OK, S. Oktyabrsky, V. Tokranov, R. Kambhampati, M. Yakimov, Y. Sun, P. Pianetta, C. Gaspe, M. Santos, J. Lee, S. Datta, P. Majhi, and W. Tsai, "Addressing The Gate Stack Challenge For High Mobility InxGaAs Channels For NFETs," *IEEE International Electron Devices Meeting Technical Digest (IEDM)*, pp. 363-366, San Francisco, California, December 2008. (Equal contribution by all authors)
- [27] S. Datta, "Sub-Quarter Volt Supply Voltage III-V Tunnel Transistors for Green Nanoelectronics," *39th IEEE Semiconductor Interface Specialists Conference (SISC)*, San Diego, California, December 2008. (Invited Talk by the candidate)
- [26] V. Saripalli\*, S. Mookerjea\*, S. Datta, and V. Narayanan, "Ultra low power signal processing architectures," *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, pp. 333-336, Baltimore, Maryland, November 2008. (First author co-supervised and second author supervised by the candidate)
- [25] S. Mookerjea\* and S. Datta, "Comparative Study of Si, Ge and InAs Based Steep Subthreshold Slope Tunnel Transistors for 0.25V Supply Voltage Logic Applications," *IEEE Device Research Conference (DRC)*, pp. 47-48, Santa Barbara, California, June 2008. (First author supervised by the candidate)
- [24] S. Datta, "Compound Semiconductor as CMOS Channel Material - Deja vu or New Paradigm?", *IEEE Device Research Conference (DRC)*, pp 33-36, Santa Barbara, California, June 2008. (Invited Talk by the candidate)
- [23] S. Eachempati, V. Saripalli\*, N. Vijaykrishnan, and S. Datta, "Reconfigurable BDD Based Quantum Circuits," *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, pp. 61-67, Anaheim, California, June 2008. (Second author co-supervised by the candidate)
- [22] S. Datta, "Enabling Green Transistors with Narrow Bandgap Ccompound Semiconductors," *32nd Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE)*, Leuven, Belgium, May 2008. (Invited Talk)
- [21] M. K. Hudait, S. Datta, G. Dewey, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, R. Pillarisetty, M. Radosavljevic, and R. Chau, "Heterogeneous Integration of Enhancement Mode In<sub>0.7</sub>Ga<sub>0.3</sub>As Quantum Well Transistor on Silicon Substrate using Thin (<2 um) Composite Buffer Architecture for High-Speed and Low-voltage (0.5V) Logic Applications," *IEEE International*



Electron Devices Meeting (IEDM) Technical Digest, pp. 625-628, Washington, D.C., December 10–12, 2007. (Equal contribution by all authors)

[20] M. Chandhok, S. Datta, D. Lionberger, and S. Vesecky, “Impact of Line Width Roughness of Intel's 65 nm Process Devices,” *Proceedings of SPIE*, pp. 6519, Orlando, Florida, 2007. (Equal contribution by all authors)

[19] J. Kavalieros, B. S. Doyle, S. Datta, and G. Dewey, “Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering,” *Digest of Technical Papers VLSI Technology Symposium*, pp. 62-63, Honolulu, Hawaii, June 15–17, 2006. (Equal contribution by all authors)

[18] S. Datta, “Antimonide based Quantum Well Transistors for High Speed, Low Power Logic Applications,” *Proceedings of the International Conference on Indium Phosphide and Related Materials (IPRM)*, pp. 174–176, Princeton, New Jersey, May 2006. (Invited talk by the candidate)

[16] S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. Phillips, D. Wallis, P. Wilding, and R. Chau, “85nm gate length enhancement and depletion mode InSb quantum well transistors for ultra high speed and very low power digital logic applications,” *International Electron Devices Meeting (IEDM) Technical Digest*, pp. 763-766, Washington, D.C., December 5-7, 2005.

[16] R. Chau, S. Datta, and A. Majumdar, “Opportunities and Challenges of III-V Nanoelectronics for Future High-speed, Low-power Logic Applications,” *IEEE Compound Semiconductor Integrated Circuit Symposium (IEEE/CSICS) Technical Digest*, pp. 17-20, Palm Springs, California, November 2005. (Equal contribution by all authors)

[15] S. Datta\* and R. Chau, “Silicon and III-V nanoelectronics,” *Proceedings on the International Conference on Indium Phosphide and Related Materials (IPRM)*, pp. 7-8, Glasgow, Scotland, May 8-12, 2005. (Invited talk by the candidate)

[14] R. Chau, J. Brask, S. Datta, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, B. Jin, M. Metz, A. Majumdar, and M. Radosavljevic, “Emerging Silicon and Non-Silicon Nano-electronic Devices: Opportunities and Challenges for Future High-Performance and Low-Power Computational Applications,” *Proceedings of Technical Papers, IEEE VLSI-TSA International Symposium on Very-large-scale integration (VLSI) Technology*, pp. 13-16, Hsinchu, Taiwan, April 2005. (Equal contribution by all authors)

- [13] T. Ashley, A. Bares, L. Buckle, S. Datta, A. Dean, M. Emeny, M. Fearn, D. Hayes, K. Hilton, R. Jefferies, T. Martin, K. Nash, T. Philips, W. Tang, P. Wilding, and R. Chau, "Novel InSb-based Quantum Well Transistors for Ultra-High Speed, Low Power Logic Applications," *Proceedings 7th International Conference on Solid-State and Integrated Circuits Technology (ICSICT)*, pp. 2253-2256, Beijing, China, October 18-21, 2004. (Equal contribution by all authors)
- [12] B. Jin, S. Datta, G. Dewey, M. Doczy, B. Doyle, K. Johnson, J. Kavalieros, M. Metz, U. Shah, N. Zelick, and R. Chau, "Mobility Enhancement in Compressively Strained SiGe Surface Channel pMOS(FET) with HfO<sub>2</sub>/TiN Gate Stack," *Proceedings of the ECS 2004 Joint International Meeting, SiGe: Materials Processing and Devices*, pp. 111-122, Hawaii, October 2004. (Equal contribution by all authors)
- [11] S. Datta, "Advanced Si and SiGe Strained NMOS and PMOS Transistors with High-K/Metal-Gate Stack," *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meetings (BCTM)*, pp. 194-197, Montreal, Canada, September 2004. (Invited talk)
- [10] S. Datta, G. Dewey, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, M. Metz, N. Zelick, and R. Chau, "High mobility Si/SiGe strained channel MOS transistors with HfO<sub>2</sub>/TiN gate stacks," *IEEE International Electron Devices Meeting (IEDM) Technical Digest*, pp. 28.1.1-28.1.4, Washington, D.C., 2003. (Equal contribution by all authors)
- [9] R. Chau, S. Datta, M. Doczy, J. Kavalieros, and M. Metz, "Gate Dielectric Scaling for High-Performance Complementary metal-oxide-semiconductor (CMOS): from SiO<sub>2</sub> to High-K," *Extended Abstracts of International Workshop on Gate Insulator (IWGI)*, pp. 124-126, Tokyo, Japan, November 2003. (Equal contribution by all authors)
- [8] R. Chau, B. Doyle, M. Doczy, S. Datta, S. Hareland, B. Jin, J. Kavalieros, and M. Metz, "Silicon Nano-Transistors and Breaking the 10nm Physical Gate Length Barrier," *Conference Digest of 61st IEEE Device Research Conference (DRC)*, pp. 123-126, Salt Lake City, Utah, June 23-25, 2003. (Equal contribution by all authors)
- [7] B. Doyle, B. Boyanov, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, R. Rios, and R. Chau, "Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout," *Digest of Technical Papers VLSI Technology Symposium*, pp. 133-134, Kyoto, Japan, June 10-12, 2003. (Equal contribution by all authors)
- [6] R. Chau, B. Doyle, J. Kavalieros, D. Barlage, A. Murthy, M. Doczy, R. Arghavani, and S. Datta, "Advanced Depleted-Substrate Transistors: Single-gate, Double-Gate and Tri-gate," *Extended*

*Abstracts of the International Conference on Solid-State Devices and Materials (SSDM)*, pp. 68-69, Nagoya, Japan, September 17-19, 2002. (Equal contribution by all authors)

[5] S. Datta, K. P. Roenker, R. E. Peddenpohl II, and M. M. Cahay, "Analysis of High Current Effects on the Performance of Pnp InP-Based Heterojunction Bipolar Transistors," *Proceedings of Twelfth International Conference on InP and Related Materials*, pp. 134-137, Piscataway, New Jersey, May 18, 2000.

[4] S. Datta, K. P. Roenker, and M. M. Cahay, "Base Pushout and High Current Effects in InP-Based Pnp Heterojunction Bipolar Transistors," *Proceedings of the State-of-the-Art Program on Compound Semiconductors XXXI, Electrochemical Society*, Vol. 99-17, Honolulu, Hawaii, October 17-19, 1999.

[3] S. Datta, K. P. Roenker, and M. M. Cahay, "High Current and Two Dimensional Effects in InP-Based Pnp Heterojunction Bipolar Transistors," *Proceedings of the State-of-the-Art Program on Compound Semiconductors XXIX, Electrochemical Society*, Vol. 98-12, Boston, Massachusetts, November 1-6, 1998.

[2] S. Datta, S. Shi, K. P. Roenker, and M. M. Cahay, "Base Design for Pnp InAlAs/InGaAs Heterojunction Bipolar Transistors," *Proceedings of the State-of-the-Art Program on Compound Semiconductors XXVI, Electrochemical Society*, Vol. 97-1, pp. 272-287, Montreal, Canada, May 4-9, 1997.

[1] S. Datta, S. Shi, K. P. Roenker, M. M. Cahay, and W. E. Stanchina, "Numerical Modeling and Design of Pnp InAlAs-InGaAs Heterojunction Bipolar Transistors," *Proceedings of the Ninth International Conference on InP and Related Materials*, pp. 392-395, Piscataway, New Jersey, May 1997.

## **Recent Invited Talks (selected)**

### **Universities**

"Steep Slope Phase Transition FETs and their applications" École Polytechnique Fédérale de Lausanne EPFL, Lausanne, Switzerland, 1/2016

"Inter-band Tunnel Transistors: Opportunities and Challenges", *NEEDS Seminar*, Purdue University, West Lafayette, IN, 10/2015

"Negative Capacitance Ferroelectric Transistors: A Promising Steep Slope Device Candidate?", *NEEDS Seminar*, Purdue University, West Lafayette, IN, 10/2015

“Ultra Low Power Devices”, *IEEE EDS Distinguished lecture series in Workshop on Connected, Autonomously Powered Systems*, Columbia University, New York, NY, 04/2014

“Cool Device Strategies for Beyond CMOS Nanoelectronics”, *ECE Colloquium*, University of Texas, Dallas, TX, 02/2014

“Cool Device Strategies for Beyond CMOS Nanoelectronics”, *ECE Colloquium*, Cornell University, Ithaca, NY, 02/2012

“Nanoelectronics for Future Energy Efficient Information Processing”, *ECE Colloquium*, University of Illinois, Urbana Champagne, IL, 03/2012

“Tunnel Transistor Based Energy Efficient Logic”, *IEEE EDS Distinguished lecture series in Electronics/Photonics*, Ohio State University, Columbus, OH, 04/2010

“Energy Efficient Logic Transistors using Compound Semiconductors” Cornell University Electron Devices Society Lecture Series, Cornell University, Ithaca, NY, 04/2010

“Logic and Memory Design using Inter-band Tunnel Transistor” Nanoseminar Seminar Series, Arizona State University, 03/2010

“Compound Semiconductor based Logic Elements” IEEE Electron Devices Mini Colloquium, Indian Institute of Technology, Mumbai, 01/2010

“Ushering in the Green Transistor Era”, Rochester Institute of Technology, Rochester, New York, 5/2009

“Green Transistors to Green Architectures”, Institut für Materialien und Bauelemente der Elektronik, Leibniz Universität Hannover (University of Hannover), Hannover, Germany, 10/2009

“Green Nanoelectronic Computing Devices”, as part of the annual workshop on Emerging Trends in Photonic and Electronic Device Research held sponsored by The University of Illinois chapters of the Optical Society of America (OSA) and the IEEE Electron Devices Society (EDS) in conjunction with the Micro and Nanotechnology Laboratory (MNTL), University of Illinois, Urbana Champagne, Illinois, 09/2008

“Recent Advances in Silicon and Non-Silicon Nanoelectronic Devices for High-Performance, Energy Efficient Logic Applications”, Penn State University Computer Science and Engineering Colloquia Series, 11/2007

“Emerging Nanoelectronic Devices for High-Speed and Ultra-Low Power Applications”, sponsored by the University of Wisconsin, Madison, Materials Research Science and Engineering

Center (MRSEC) in association with Electrical Engineering Department University of Wisconsin, Madison, Wisconsin, 12/2006

“Ultra Low Power Nanoelectronics for the Logic technology”, Taipei Local Chapter of IEEE Electron Devices Society (EDS), National Tshao-tung University (NCTU), Hsinshu, Taiwan, 12/2006

“Emerging Nanoelectronic Devices for High-Speed and Ultra-Low Power Application”, Electrical Engineering Colloquium, University of Texas, Austin, 3/2006

“Silicon Nano-Transistors and Nanotechnology for High-Performance Logic Applications”, sponsored by the IEEE Phoenix Section Components, Packaging, and Manufacturing Technology Society Chapter, & Waves and Devices Chapter, Arizona State University, Tempe, Arizona, 11/2003

### **Government/Industry**

“Steep Slope Transistors”, Speaker at the IEEE Rebooting Computing Workshop, Washington DC, 10/12/2015

“Steep Slope Transduction FETs”, Invited Speaker at Global Foundries, Malta, New York, 10/21/2015

“Strained Germanium Quantum Well FinFETs”, Invited Speaker at Global Foundries, Malta, New York, 09/01/2015

“Steep Slope Transistors”, Keynote Speaker at the NSF sponsored “The Workshop for Energy Efficient Computing” Arlington, VA, 04/14/2015

“Function Stacks for Logic and Memory Devices”, Invited Speaker at the SEMATECH's 7th International Symposium on Advanced Gate Stack Technology, in Albany, New York, 09/29/2010-10/01/2010

“Non silicon logic elements for extreme voltage scaling “, Invited Speaker at the IBM MRC Workshop on III/V Devices IBM Research, Zurich, Switzerland, 09/2010

“Binary Decision Diagram Logic for Single Electron Devices and Tunnel FETs”, Invited Speaker at the Nanoelectronics Research Initiative (NRI) sponsored Architecture & Device Benchmarking Workshop, University of Notre Dame, 08/09/2010

“Tunnel Transistors: From Circuits to Architecture”, Invited Speaker at the Nanoelectronics Research Initiative (NRI) sponsored Architecture & Device Benchmarking Workshop, University of Notre Dame, 08/09/2010

“High mobility channel MOSFETs: to include or not to include in the ITRS?”, Panelist at the Sematech/IMEC III-V Workshop for discussion on inclusion high mobility channel MOSFETs in the ITRS, Hilton Hawaiian Village, Honolulu, 06/2010

“Green Transistors to Green Architectures”, Tutorial at the 16th IEEE International Symposium on High-Performance Computer Architecture (HPCA), Bangalore, India, 01/2010

“High Mobility Channel MOSFETs”, Panelist at the Workshop for Future III-V Complementary Metal–Oxide–Semiconductor (CMOS) Technology, Washington DC , December 2009

“Heterojunction Tunnel Transistor Logic,” Intel on-site NRI sponsored PI’s Workshop, Intel Corporation, Portland, Oregon, 8/2009

“Tunnel Transistor Logic”, Intel Microprocessor Research Lab Seminar, Portland, Oregon, 10/09

"Looking Beyond Silicon - A Pipe Dream or the Inevitable Next Step?" Panelist on the IEDM sponsored evening panel called (This panel assembled internationally recognized panelists to discuss the future of Complementary Metal-Oxide Semiconductor (CMOS) and beyond CMOS for leading-edge advanced integrated circuit applications”, 12/2007

"III-V Complementary Metal-Oxide Semiconductor (CMOS) on Si: Technical and Manufacturing Needs” Panelist on the Sematech and Aixtron sponsored workshop on readiness of III-V MOSFET Technology. This workshop received world-wide press coverage under the heading “III-V Compounds Emerging as Prime Materials for Future NMOS Channels, Technologists Indicate at SEMATECH & AIXTRON Workshop,” Washington, D.C., 12/2007

## **Inventions**

[164] US Patent # 9048314 “Field effect transistor with narrow bandgap source and drain regions and method of fabrication”

[163] US Patent # 9006707 “Forming arsenide-based complementary logic on a single substrate”

[162] US Patent # 8841180 “Strain-inducing semiconductor regions”

[161] US Patent # 8816394 “Field effect transistor with narrow bandgap source and drain regions and method of fabrication”

[160] US Patent # 8803255 “Gate electrode having a capping layer ”

[159] US Patent # 8802517 “Extreme high mobility CMOS logic ”

[158] US Patent # 8664694 “Field effect transistor with narrow bandgap source and drain regions and method of fabrication”

- [157] US Patent # 8638591 “TFET based 4T memory devices”
- [156] US Patent # 8581258 “Semiconductor device structures and methods of forming semiconductor structures”
- [155] US Patent # 8530884 “Strain inducing semiconductor regions”
- [154] US Patent # 8518768 “Extreme high mobility CMOS logic”
- [153] US Patent # 8421059 “Strain inducing semiconductor region”
- [152] US Patent # 8405164 “Tri-gate transistor device with stress incorporation layer and method of fabrication ”
- [151] US Patent # 8390082 “Gate electrode having a capping layer ”
- [150] US Patent # 8369134 “TFET based 6T SRAM cell ”
- [149] US Patent # 8368135 “Field effect transistor with narrow bandgap source and drain regions and method of fabrication”
- [148] US Patent # 8294180 “CMOS devices with a single work function gate electrode and method of fabrication”
- [147] US Patent # 8288233 “Method to introduce uniaxial strain in multigate nanoscale transistors by self aligned SI to SIGE conversion processes and structures formed thereby ”
- [146] US Patent # 8273626 “Nonplanar semiconductor device with partially or fully wrapped around gate electrode and methods of fabrication”
- [145] US Patent # 8264004 “Mechanism for forming a remote delta doping layer of a quantum well structure”
- [144] US Patent # 8237234 “Transistor gate electrode having conductor material layer”
- [143] US Patent # 8232588 “Increasing the surface area of a memory cell capacitor”
- [142] US Patent # 8217383 “High hole mobility p-channel Ge transistor structure on Si substrate”
- [141] US Patent # 8193567 “Process for integrating planar and non-planar CMOS transistors on a bulk substrate and article made thereby ”
- [140] US Patent # 8183646 “Field effect transistor with narrow bandgap source and drain regions and method of fabrication ”
- [139] US Patent # 8183556 “Extreme high mobility CMOS logic”
- [138] US Patent # 8169027 “Substrate band gap engineered multi-gate pMOS devices”

- [137] US Patent # 8148786 “Complementary metal oxide semiconductor integrated circuit using raised source drain and replacement metal gates”
- [136] US Patent # 8138042 “Capacitor, method of increasing a capacitance area of same, and system containing same”
- [135] US Patent # 8129795 “Inducing strain in the channels of metal gate transistors”
- [134] US Patent # 8124959 “High hole mobility semiconductor device”
- [133] US Patent # 8120065 “Tensile strained NMOS transistor using group III-N source/drain regions”
- [132] US Patent # 8119508 “Forming integrated circuits with replacement metal gate electrodes”
- [131] US Patent # 8084818 “High mobility tri-gate devices and methods of fabrication”
- [130] US Patent # 8071983 “Semiconductor device structures and methods of forming semiconductor structures,” J. Brask, J. Kavalieros, U. Shah, S. Datta, A. Majumdar, R. Chau, B. Doyle, Dec 06, 2011
- [129] US Patent # 79892807 “Dielectric interface for group III-V semiconductor device,” J. Brask, S. Datta, M. Doczy, J. Blackwell, M. Metz, J. Kavalieros, R. Chau, Aug 02, 2011
- [128] US Patent # 7968957 “Transistor gate electrode having conductor material layer,” A. Murthy, B. Boyanov, S. Datta, B. Doyle, B. Jin, S. Yu, R. Chau, June 28, 2011
- [127] US Patent # 7960794 “Non-planar pMOS structure with a strained channel region and an integrated strained CMOS flow,” B. Doyle, S. Datta, B. Jin, N. Zelick, R. Chau, June 14, 2011
- [126] US Patent # 7951673 “Forming abrupt source drain metal gate transistors,” N. Lindert, S. Datta, J. Kavalieros, M. Doczy, M. Metz, J. Brask, R. Chau, M. Bohr, A. Murthy, May 31, 2011
- [125] US Patent # 7915694 “Gate electrode having a capping layer,” G. Dewey, M. Doczy, S. Datta, J. Brask, M. Metz, Mar 29, 2011
- [124] US Patent # 7915167 “Fabrication of channel wraparound gate structure for field-effect transistor,” M. Radosavljevic, A. Majumdar, B. Doyle, J. Kavalieros, M. Doczy, J. Brask, U. Shah, S. Datta, R. Chau, Mar 29, 2011
- [124] US Patent # 7902058 “Inducing strain in the channels of metal gate transistors,” S. Datta, J. Kavalieros, M. Doczy, M. Metz, J. Brask, R. Chau, B. Doyle, Mar 08, 2011



- [123] US Patent # 7902014 “CMOS devices with a single work function gate electrode and method of fabrication,” B. Doyle, B. Jin, J. Kavalieros, S. Datta, J. Brask, R. Chau, Mar 08, 2011
- [122] US Patent # 7898041 “Block contact architectures for nanoscale channel transistors,” M. Radosavljevic, A. Majumdar, B. Doyle, J. Kavalieros, M. Doczy, J. Brask, U. Shah, S. Datta, R. Chau, Mar 01 , 2011
- [121] US Patent # 7893506 “Field effect transistor with narrow bandgap source and drain regions and method of fabrication,” R. Chau, S. Datta, J. Kavalieros, J. Brask, M. Doczy, M. Metz, Feb 22, 2011
- [120] US Patent # 7888221 “Tunneling field effect transistor using angled implants for forming asymmetric source/drain regions,” J. Kavalieros. M. Metz, G. Dewey, B. Jin, J. Brask, S. Datta, R. Chau, Feb 15, 2011
- [119] US Patent # 7883951 “CMOS device with metal and silicide gate electrodes and a method for making it,” J. Brask, M. Doczy, J. Kavalieros, M. Metz, C. Barns, U. Shah, S. Datta, C. Thomas, R. Chau, Feb 08, 2011
- [118] US Patent # 7879739 “Thin transition layer between a group III-V substrate and a high-k gate dielectric layer,” W. Rachmady, J. Blackwell, S. Datta, J. Kavalieros, M. Hudait, Feb 01, 2011
- [117] US Patent # 7879675 “Field effect transistor with metal source/drain regions,” M. Radosavljevic, S. Datta, B. Doyle, J. Kavalieros, J. Brask, M. Doczy, A. Majumdar, R. Chau, Feb 01, 2011
- [116] US Patent # 7875937 “Semiconductor device with a high-k gate dielectric and a metal gate electrode,” M. Metz, M. Doczy, J. Brask, J. Kavalieros, R. Chau, Robert S, Jan 25, 2011
- [115] US Patent # 7871916 “Transistor gate electrode having conductor material layer,” A. Murthy, B. Boyanov, S. Datta, B. Doyle, B. Jin, S. Yu, R. Chau, Jan 18, 2011
- [114] US Patent # 7859081 “Capacitor, method of increasing a capacitance area of same, and system containing same,” B. Doyle, R. Chau, S. Datta, V. De, A. Keshavarzi, D. Somasekhar, Dec 28, 2010
- [113] US Patent # 7858481 “Method for fabricating transistor with thinned channel,” J. Brask, R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, A. Majumdar, M. Metz, M. Radosavljevic, Dec 28, 2010

- [112] US Patent # 7825481 "Field effect transistor with narrow bandgap source and drain regions and method of fabrication," R. Chau, S. Datta, J. Kavalieros, J. Brask, M. Doczy, M. Metz, Nov 02, 2010
- [111] US Patent # 7825437 "Unity beta ratio tri-gate transistor static random access memory (SRAM)," R. Pillarisetty, S. Datta, J. Kavalieros, B. Doyle, U. Shah, Nov 02, 2010
- [110] US Patent # 7825400 "Strain-inducing semiconductor regions," S. Datta, J. Kavalieros, B. Jin, Nov 02, 2010
- [109] US Patent # 7820513 "Nonplanar semiconductor device with partially or fully wrapped around gate electrode and methods of fabrication," S. Hareland, R. Chau, B. Doyle, R. Rios, T. Linton, S. Datta, Oct 26, 2010
- [108] US Patent # 7820512 "Spacer patterned augmentation of tri-gate transistor gate length," R. Pillarisetty, S. Datta, J. Kavalieros, B. Doyle, U. Shah. Oct 26, 2010
- [107] US Patent # 7791063 "High hole mobility p-channel Ge transistor structure on Si substrate," M. Hudait, S. Datta, J. Kavalieros, P. Tolchinsky, Sept 07, 2010
- [106] US Patent # 7790536 8 "Dopant confinement in the delta doped layer using a dopant segregation barrier in quantum well structures" M. Hudait, A. Budrevich, D. Loubychev, J. Kavalieros, S. Datta, J. Fastenau, A. Liu Sept 07, 2010
- [105] US Patent # 7785958 "Method for making a semiconductor device having a high-k gate dielectric layer and a metal gate electrode," M. Doczy, J. Brask, J. Kavalieros, U. Shah, M. Metz, S. Datta, R. Nagisetty, R. Chau, Aug 31, 2010.
- [104] US Patent # 7776684 "Increasing the surface area of a memory cell capacitor," B. Doyle, R. Chau, V. De, D. Somasekhar, Aug 17, 2010.
- [103] US Patent # 7736956 "Lateral undercut of metal gate in SOI device," S. Datta, J. Brask, J. Kavalieros, B. Doyle, G. Dewey, M. Doczy, R. Chau, June 15, 2010.
- [102] US Patent # 7718479 "Forming integrated circuits with replacement metal gate electrodes," J. Kavalieros, J. Brask, M. Doczy, M. Metz, S. Datta, U. Shah, R. Chau, May 18, 2010.
- [101] US Patent # 7714397 "Tri-gate transistor device with stress incorporation layer and method of fabrication," S. Hareland, R. Chau, B. Doyle, S. Datta, B. Jin, May 11, 2010.
- [100] US Patent # 7713803 "Mechanism for forming a remote delta doping layer of a quantum well structure," B. Jin, J. Kavalieros, S. Datta, A. Majumdar, R. Chau, B. Jin, May 11, 2010

- [99] US Patent # 7709909 "Method for making a semiconductor device having a high-k gate dielectric," M. Doczy, G. Dewey, S. Datta, S. Pae, J. Brask, J. Kavalieros, M. Metz, A. Sherrill, M. Kuhn, R. Chau, May 04, 2010.
- [98] US Patent # 7704833 "Method of forming abrupt source drain metal gate transistor," N. Lindert, S. Datta, J. Kavalieros, M. Doczy, M. Metz, J. Brask, R. Chau, M. Bohr, A. Murthy, April 27, 2010.
- [97] US Patent # 7671471 "Method for making a semiconductor device having a high-k dielectric layer and a metal gate electrode," J. Brask, J. Kavalieros, M. Doczy, U. Shah, C. Barnes, M. Metz, S. Datta, A. Cappellani, R. Chau, March 03, 2010.
- [96] US Patent # 7642610 "Transistor gate electrode having conductor material layer," A. Murthy, B. Boyanov, S. Datta, B. Doyle, B. Jin, S. Yu, R. Chau, January 05, 2010.
- [95] US Patent # 7642603 "Semiconductor device with reduced fringe capacitance," S. Datta, T. Rakshit, J. Kavalieros, B. Doyle, January 05, 2010.
- [94] US Patent # 7638169 "Directing carbon nanotube growth," M. Radosavljevic, J. Kavalieros, A. Majumdar, S. Datta, December 29, 2009.
- [93] US Patent # 7629643 "Independent n-tips for multi-gate transistors," R. Pillarisetty, S. Datta, J. Kavalieros, B. Doyle, December 12, 2009
- [92] US Patent # 7615441 "Forming high-k dielectric layers on smooth substrates," J. Brask, J. Kavalieros, M. Doczy, M. Metz, S. Datta, U. Shah, G. Dewey, R. Chau, November 10, 2009
- [91] US Patent # 7608883 "Transistor for non volatile memory devices having a carbon nanotube channel and electrically floating quantum dots in its gate dielectric" M. Radosavljevic, A. Majumdar, S. Datta, J. Brask, B. Doyle, R. Chau, October 27, 2009
- [90] US Patent # 7601980 "Dopant confinement in the delta doped layer using a dopant segregation barrier in quantum well structures" M. Hudait, A. Budrevich, D. Loubychev, J. Kavalieros, S. Datta, J. Fastenau, A. Liu, October 13, 2009
- [89] US Patent # 7598560 "Hetero-bimos injection process for non-volatile flash memory," J. Kavalieros, S. Datta, R. Chau, D. Kencke, October 6, 2009.
- [88] US Patent # 7592213 "Tensile strained NMOS transistor using group III-N source/drain regions," S. Datta, J. Brask, B. Jin, J. Kavalieros, M. Hudait, September 22, 2009.
- [87] US Patent # 7575991 "Removing a high-k gate dielectric," M. Doczy, R. Norman, J. Brask, M. Metz, S. Datta, R. Chau, August 18, 2009.

- [86] US Patent # 7569857 "Dual crystal orientation circuit devices on the same substrate," P. Tolchinsky, J. Kavalieros, B. Doyle, S. Datta, August 4, 2009.
- [85] US Patent # 7569869 "Transistor having tensile strained channel and system including same," B. Jin, R. Chau, S. Datta, J. Kavalieros, M. Radosavljevic, August 4, 2009.
- [84] US Patent # 7566898 "Buffer architecture formed on a semiconductor wafer," M. Hudait, D. Loubychev, S. Datta, R. Chau, J. Fastenau, A. Liu, July 28, 2009.
- [83] US Patent # 7560756 "Tri-gate devices and methods of fabrication," R. Chau, B. Doyle, J. Kavalieros, D. Barlage, S. Datta, July 14, 2009.
- [82] US Patent # 7547637 "Methods for patterning a semiconductor film," J. Brask, J. Kavalieros, U. Shah, S. Datta, A. Majumdar, R. Chau, B. Doyle, June 16, 2009.
- [81] US Patent # 7531393 "Non-planar MOS structure with a strained channel region," B. Doyle, S. Datta, B. Jin, R. Chau, May 12, 2009.
- [80] US Patent # 7531404 "Semiconductor device having a metal gate electrode formed on an annealed high-k gate dielectric layer," S. Pae, J. Maiz, J. Brask, G. Dewey, J. Kavalieros, R. Chau, S. Datta, May 12, 2009.
- [79] US Patent # 7524727 "Gate electrode having a capping layer," G. Dewey, M. Doczy, S. Datta, J. Brask, M. Metz, April 28, 2009.
- [78] US Patent # 7525160 "Multigate device with recessed strain regions," J. Kavalieros, J. Brask, S. Datta, B. Doyle, R. Chau, April 28, 2009
- [77] US Patent # 7514346 "Tri-gate devices and methods of fabrication," R. Chau, B. Doyle, J. Kavalieros, D. Barlage, S. Datta, April 14, 2009.
- [76] US Patent # 7518196 "Field effect transistor with narrow bandgap source and drain regions and method of fabrication," R. Chau, S. Datta, J. Kavalieros, J. Brask, M. Metz, April 14, 2009.
- [75] US Patent # 7514746 "Floating-body dynamic random access memory and method of fabrication in tri-gate technology," S. Tang, A. Keshavarzi, D. Somasekhar, F. Paillet, M. Khellah, Y. Ye, S. Lu, B. Doyle, S. Datta, V. De, April 7, 2009.
- [74] US Patent # 7504678 "Tri-gate devices and methods of fabrication," R. Chau, B. Doyle, J. Kavalieros, D. Barlage, S. Datta, March 17, 2009.
- [73] US Patent # 7501336 "Metal gate device with reduced oxidation of a high-k gate dielectric," B. Doyle, J. Kavalieros, J. Brask, M. Metz, M. Doczy, S. Datta, R. Chau, March 10, 2009.

- [72] US Patent # 7569443 “Complementary metal oxide semiconductor integrated circuit using raised source drain and replacement metal gate,” J. Kavalieros, A. Cappellani, J. Brask, M. Doczy, S. Datta, C. Barnes, R. Chau, January 20, 2009.
- [71] US Patent # 7494862 “Methods for uniform doping of non-planar transistor structures,” B. Doyle, R. Chau, S. Datta, J. Kavalieros, February 24, 2009.
- [70] US Patent # 7485503 “Dielectric interface for group III-V semiconductor device,” J. Brask, S. Datta, M. Doczy, J. Blackwell, M. Metz, J. Kavalieros, R. Chau, February 3, 2009.
- [69] US Patent # 7479421 “Process for integrating planar and non-planar CMOS transistors on a bulk substrate and article made thereby,” J. Kavalieros, J. Brask, B. Doyle, U. Shah, S. Datta, M. Doczy, M. Metz, R. Chau, January 20, 2009.
- [68] US Patent # 7465976 “Tunneling field effect transistor using angled implants for forming asymmetric source/drain regions,” J. Kavalieros, M. Metz, G. Dewey, B. Jin, S. Datta, R. Chau, December 16, 2008.
- [67] US Patent # 7456476 “Nonplanar semiconductor device with partially or fully wrapped around gate electrode and methods of fabrication,” S. Hareland, R. Chau, B. Doyle, R. Rios, T. Linton, S. Datta, November 25, 2008.
- [64] US Patent # 7449373 “Method of ion implanting for tri-gate devices,” B. Doyle, S. Datta, J. Kavalieros, A. Majumdar, November 11, 2008.
- [63] US Patent # 7449756 “Semiconductor device with a high-k gate dielectric and a metal gate electrode or fully wrapped around gate electrode and methods of fabrication,” M. Metz, S. Datta, M. Doczy, J. Brask, J. Kavalieros, R. Chau, November 11, 2008.
- [62] US Patent # 7445980 “Method and apparatus for improving stability of a 6T CMOS SRAM cell,” S. Datta, B. Doyle, R. Chau, B. Jin, J. Kavalieros, B. Zheng, S. Hareland, November 4, 2008.
- [61] US Patent # 7442983 “Method for making a semiconductor device having a high-k gate dielectric,” M. Doczy, G. Dewey, S. Datta, S. Pae, J. Brask, J. Kavalieros, M. Metz, A. Sherrill, M. Kuhn, R. Chau, October 28, 2008.
- [60] US Patent # 7439113 “Forming dual metal complementary metal oxide semiconductor integrated circuits,” M. Doczy, M. Taylor, J. Brask, J. Kavalieros, S. Datta, M. Metz, R. Chau, J. Hwang, October 21, 2008.
- [59] US Patent # 7427794 “Tri-gate devices and methods of fabrication,” R. Chau, B. Doyle, J. Kavalieros, D. Barlage, S. Datta, S. Hareland, September 23, 2008.

- [58] US Patent # 7429747 "Sb-based CMOS devices," M. Hudait, S. Datta, J. Kavalieros, M. Doczy, R. Chau, September 30, 2008.
- [57] US Patent # 7427541 "Carbon nanotube energy well (CNEW) field effect transistor," S. Datta, M. Radosavljevic, B. Doyle, J. Kavalieros, J. Brask, A. Majumdar, R. Chau, September 23, 2008.
- [56] US Patent # 7425490 "Reducing reactions between polysilicon gate electrodes and high dielectric constant gate dielectrics," J. Kavalieros, J. Brask, M. Doczy, U. Shah, M. Metz, S. Datta, R. Chau, September 16, 2008.
- [55] US Patent # 7425500 "Uniform silicide metal on epitaxially grown source and drain regions of three-dimensional transistors," M. Metz, S. Datta, J. Kavalieros, M. Doczy, J. Brask, R. Chau, September 16, 2008.
- [54] US Patent # 7407847 "Stacked multi-gate transistor design and method of fabrication," B. Doyle, T. Rakshit, R. Chau, S. Datta, J. Brask, U. Shah, August 5, 2008.
- [53] US Patent # 7402875 "Lateral undercut of metal gate in SOI device," S. Datta, J. Brask, J. Kavalieros, B. Doyle, G. Dewey, M. Doczy, R. Chau, July 22, 2008.
- [52] US Patent # 7390947 "Forming field effect transistors from conductors," A. Majumdar, J. Brask, M. Radosavljevic, S. Datta, B. Doyle, M. Doczy, J. Kavalieros, M. Metz, R. Chau, U. Shah, J. Blackwell, June 24, 2008.
- [51] US Patent # 7390709 "Method for making a semiconductor device having a high-k gate dielectric layer and a metal gate electrode," M. Doczy, J. Brask, J. Kavalieros, U. Shah, M. Metz, S. Datta, R. Nagisetty, R. Chau, June 24, 2008.
- [50] US Patent # 7387927 "Reducing oxidation under a high K gate dielectric," R. Turkot, J. Brask, J. Kavalieros, M. Doczy, M. Metz, U. Shah, S. Datta, R. Chau, June 17, 2008.
- [49] US Patent # 7384880 "Method for making a semiconductor device having a high-k gate dielectric," J. Brask, J. Kavalieros, M. Doczy, S. Datta, R. Chau, June 10, 2008.
- [48] US Patent # 7381608 "Method for making a semiconductor device with a high-k gate dielectric and a metal gate electrode," J. Brask, S. Pae, J. Kavalieros, M. Metz, M. Doczy, S. Datta, R. Chau, J. Maiz, June 03, 2008.
- [47] US Patent # 7358121 "Tri-gate devices and methods of fabrication," R. Chau, B. Doyle, J. Kavalieros, D. Barlage, S. Datta, April 15, 2008.

- [46] US Patent # 7355281 "Method for making semiconductor device having a high-k gate dielectric layer and a metal gate electrode," J. Brask, J. Kavalieros, M. Doczy, U. Shah, C. Barnes, M. Metz, S. Datta, A. Cappellani, R. Chau, April 08, 2008.
- [45] US Patent # 7355254 "Pinning layer for low resistivity N-type source drain ohmic contacts," S. Datta, J. Kavalieros, M. Doczy, R. Chau, April 08, 2008.
- [44] US Patent # 7348284 "Non-planar pMOS structure with a strained channel region and an integrated strained CMOS flow," B. Doyle, S. Datta, B. Jin, N. Zelick, R. Chau, March 25, 2008.
- [43] US Patent # 7342277 "Transistor for non volatile memory devices having a carbon nanotube channel and electrically floating quantum dots in its gate dielectric," M. Radosavljevic, A. Majumdar, S. Datta, J. Brask, B. Doyle, R. Chau, March 11, 2008.
- [42] US Patent #7323423 "Forming high-k dielectric layers on smooth substrates," J. Brask, J. Kavalieros, M. Doczy, M. Metz, S. Datta, U. Shah, G. Dewey, R. Chau, January 29, 2008.
- [41] US Patent #7317231 "Method for making a semiconductor device having a high-K gate dielectric and a titanium carbide gate electrode," M. Metz, S. Datta, M. Doczy, J. Kavalieros, J. Brask, R. Chau, January 8, 2008.
- [40] US Patent #7279375 "Block contact architectures for nanoscale channel transistors," M. Radosavljevic, A. Majumdar, B. Doyle, J. Kavalieros, M. Doczy, J. Brask, U. Shah, S. Datta, R. Chau, October 9, 2007.
- [39] US Patent # 7268058 "Tri-gate transistors and methods to fabricate same," R. Chau, S. Datta, B. Doyle, B. Jin, September 11, 2007.
- [38] US Patent # 7241653 "Nonplanar device with stress incorporation layer and method of fabrication," S. Hareland, R. Chau, B. Doyle, S. Datta, B. Jin, July 10, 2007.
- [37] US Patent # 7235809 "Semiconductor channel on insulator structure," B. Jin, B. Doyle, S. Hareland, M. Doczy, M. Metz, B. Boyanov, S. Datta, J. Kavalieros, R. Chau, June 26, 2007.
- [36] US Patent # 7223679 "Transistor gate electrode having conductor material layer," A. Murthy, B. Boyanov, S. Datta, B. Doyle, B. Jin, S. Yu, R. Chau, May 29, 2007.
- [35] US Patent #7220635 "Method for making a semiconductor device with a metal gate electrode that is formed on an annealed high-k gate dielectric layer," J. Brask, M. Doczy, J. Kavalieros, U. Shah, M. Metz, C. Barnes, S. Datta, C. Thomas, R. Chau, May 22, 2007.
- [34] US Patent # 7193279 "Non-planar MOS structure with a strained channel region," B. Doyle, S. Datta, B. Jin, R. Chau, March 20, 2007.

- [33] US Patent # 7192890 “Depositing an oxide,” Y. Zhou, M. Metz, J. Brask, J. Burghard, M. Kuhn, S. Datta, R. Chau, March 20, 2007.
- [32] US Patent #719285 “Forming dual metal complementary metal oxide semiconductor integrated circuits,” M. Doczy, L. Wong, V. Dubin, J. Brask, J. Kavalieros, S. Datta, M. Metz, R. Chau, March 20, 2007.
- [31] US Patent #7176090 “Method for making a semiconductor device that includes a metal gate electrode,” J. Brask, J. Kavalieros, M. Doczy, M. Metz, S. Datta, U. Shah, B. Doyle, R. Chau, February 13, 2007.
- [30] US Patent #7170120 “Carbon nanotube energy well (CNEW) field effect transistor,” S. Datta, M. Radosavljevic, B. Doyle, J. Kavalieros, J. Brask, A. Majumdar, R. Chau, January 30, 2007.
- [29] US Patent #7160779 “Method for making a semiconductor device having a high-k gate dielectric,” M. Doczy, J. Kavalieros, J. Brask, M. Metz, S. Datta, B. Doyle, R. Chau, January 9, 2007.
- [28] US Patent #7157378 “Method for making a semiconductor device having a high-k gate dielectric layer and a metal gate electrode,” J. Brask, C. Barns, M. Doczy, U. Shah, J. Kavalieros, M. Metz, S. Datta, A. Miller, R. Chau, January 2, 2007.
- [27] US Patent #7153784 “Method for making a semiconductor device having a high-k gate dielectric layer and a metal gate electrode,” J. Brask, J. Kavalieros, M. Doczy, U. Shah, C. Barns, M. Metz, S. Datta, A. Cappellani, R. Chau, December 26, 2006.
- [26] US Patent #7153734 “CMOS device with metal and silicide gate electrodes and a method for making it,” Brask, Justin K. (Portland, OR, US) M. Doczy, J. Kavalieros, M. Metz, C. Barns, U. Shah, S. Datta, C. Thomas, R. Chau, December 26, 2006.
- [25] US Patent #7148548 “Semiconductor device with a high-k gate dielectric and a metal gate electrode,” M. Doczy, J. Kavalieros, M. Metz, J. Brask, S. Datta, R. Chau, December 12, 2006.
- [24] US Patent #7148099 “Reducing the dielectric constant of a portion of a gate dielectric,” S. Datta, J. Kavalieros, M. Doczy, M. Metz, J. Brask, R. Chau, December 12, 2006.
- [23] US Patent #7144783 “Reducing gate dielectric material to form a metal gate electrode extension,” S. Datta, J. Brask, J. Kavalieros, M. Doczy, M. Metz, R. Chau, December 5, 2006.
- [22] US Patent #7138323 “Planarizing a semiconductor structure to form replacement metal gates,” J. Kavalieros, J. Brask, M. Doczy, U. Shah, C. Barns, M. Metz, S. Datta, R. Chau, November 21, 2006.



- [21] US Patent #7138316 "Semiconductor channel on insulator structure," B. Jin, B. Doyle, S. Hareland, M. Doczy, M. Metz, Matthew, B. Boyanov, S. Datta, J. Kavalieros, R. Chau, November 21, 2006.
- [20] US Patent #7138305 "Method and apparatus for improving stability of a 6T CMOS SRAM cell," S. Datta, B. Doyle, R. Chau, J. Kavalieros, B. Zheng, S. Hareland, November 21, 2006.
- [19] US Patent #7126199 "Multilayer metal gate electrode," M. Doczy, J. Brask, J. Kavalieros, C. Barns, M. Metz, S. Datta, R. Chau, October 24, 2006.
- [18] US Patent #7125762 "Compensating the workfunction of a metal gate transistor for abstraction by the gate dielectric layer," J. Brask, J. Kavalieros, M. Doczy, M. Metz, S. Datta, U. Shah, R. Chau, October 24, 2006.
- [17] US Patent #7098507 "Floating-body dynamic random access memory and method of fabrication in tri-gate technology," S. Tang, A. Keshavarzi, D. Somasekhar, F. Paillet, M. Khellah, Y. Ye, S. Lu, B. Doyle, S. Datta, V. De, August 29, 2006.
- [16] US Patent #7087476 "Using different gate dielectrics with NMOS and PMOS transistors of a complementary metal oxide semiconductor integrated circuit," M. Metz, S. Datta, J. Kavalieros, M. Doczy, J. Brask, R. Chau, August 8, 2006.
- [15] US Patent #7084038 "Method for making a semiconductor device having a high-k gate dielectric," M. Doczy, G. Dewey, S. Datta, S. Pae, J. Brask, J. Kavalieros, M. Metz, A. Sherrill, M. Kuhn, R. Chau, August 1, 2006.
- [14] US Patent #7074680 "Method for making a semiconductor device having a high-k gate dielectric," M. Doczy, G. Dewey, S. Datta, S. Pae, J. Brask, J. Kavalieros, M. Metz, Matt, A. Sherrill, M. Kuhn, R. Chau, July 11, 2006.
- [13] US Patent #7064066 "Method for making a semiconductor device having a high-k gate dielectric and a titanium carbide gate electrode," M. Metz, S. Datta, M. Doczy, J. Kavalieros, J. Brask, R. Chau, June 20, 2006.
- [12] US Patent #7060568 "Using different gate dielectrics with NMOS and PMOS transistors of a complementary metal oxide semiconductor integrated circuit," M. Metz, S. Datta, J. Kavalieros, M. Doczy, J. Brask, R. Chau, June 13, 2006.
- [11] US Patent #7045428 "Method for making a semiconductor device with a high-k gate dielectric and a conductor that facilitates current flow across a P/N junction," J. Brask, J. Kavalieros, M. Doczy, M. Metz, U. Shah, C. Barns, S. Datta, R. Turkot, R. Chau, May 16, 2006.

- [10] US Patent #7042009 “High mobility tri-gate devices and methods of fabrication,” M. Shaheen, B. Doyle, S. Datta, R. Chau, P. Tolchinsky, May 9, 2006.
- [9] US Patent #7005366 “Tri-gate devices and methods of fabrication,” R. Chau, B. Doyle, J. Kavalieros, D. Barlage, S. Datta, S. Hareland, February 28, 2006.
- [8] US Patent #6974738 “Nonplanar device with stress incorporation layer and method of fabrication,” S. Hareland, R. Chau, B. Doyle, S. Datta, December 13, 2005.
- [7] US Patent #6970373 “Method and apparatus for improving stability of a 6T CMOS SRAM cell,” S. Datta, B. Doyle, R. Chau, J. Kavalieros, B. Zheng, S. Hareland, November 29, 2005.
- [6] US Patent #6787440 “Method for making a semiconductor device having an ultra-thin high-k gate dielectric,” C. Parker, M. Kuhn, Y. Zhou, S. Hareland, S. Datta, N. Lindert, R. Chau, T. Glassman, M. Metz, S. Tyagi, September 7, 2005.
- [5] US Patent #6914295 “Tri-gate devices and methods of fabrication,” R. Chau, B. Doyle, J. Kavalieros, D. Barlage, S. Datta, S. Hareland, July 5, 2005.
- [4] US Patent #6909151 “Nonplanar device with stress incorporation layer and method of fabrication,” S. Hareland, R. Chau, B. Doyle, S. Datta, B. Jin, June 21, 2005.
- [3] US Patent #6887800 “Method for making a semiconductor device with a high-k gate dielectric and metal layers that meet at a P/N junction,” M. Metz, S. Datta, J. Kavalieros, M. Doczy, J. Brask, U. Shah, R. Chau, May 3, 2005.
- [2] US Patent #6869889 “Etching metal carbide films,” J. Brask, J. Kavalieros, M. Doczy, M. Metz, S. Datta, U. Shah, T. Bacuita, R. Chau, March 22, 2005.
- [1] US Patent #6858478 “Tri-gate devices and methods of fabrication,” R. Chau, B. Doyle, J. Kavalieros, D. Barlage, S. Datta, S. Hareland, February 22, 2005.

## **Professional Activities**

**Distinguished Lecturer**, Electron Devices Society, IEEE

**Fellow**, IEEE

**Member**, *Executive Committee, Electronics and Photonics Division, the Electrochemical Society (ECS)*, September 2009-present

**Member**, *Executive Committee, Mid-West Institute for Nanoelectronics Discovery (MIND)*, 2008-2012

**Member**, *Executive Committee, Center for Low Energy Systems Technology (LEAST)*, 2013-present

**Member**, “*Front End Processes*” *Tab and contributor to the 2003 Version of the International Technology Roadmap for Semiconductors (ITRS)*

**Member**, *American Society for Engineering Education*, 2007 – Present

**Vice Chair**, *Short Course, IEEE International Electron Devices Meeting (IEDM '15)*, Washington DC, December 2016

**Chair**, *Publications, IEEE International Electron Devices Meeting (IEDM '15)*, Washington DC, December 2015

**TPC Member**, *Design Automation Conference (DAC '16)*, San Francisco

**TPC Member**, *International Conference on Simulation of Semiconductor Processes & Devices (SISPAD '16)*, Dresden, Germany

**TPC Member**, *International Reliability Physics Symposium (IRPS '16)*

**Chair**, *Publicity, IEEE International Electron Devices Meeting (IEDM '14)*, San Francisco, California, December 2014

**Chair**, *Tutorials, IEEE International Electron Devices Meeting (IEDM '12)*, San Francisco, California, December 2012

**General Chair**, *IEEE Device Research Conference (DRC)*, Notre Dame University, University Park, PA, June 2013

**Program Chair**, *IEEE Device Research Conference (DRC)*, Pennsylvania State University, University Park, PA, June 2012

**Chair**, *Emerging Technologies, IEEE International Electron Devices Meeting (IEDM '11)*, Washington DC, December 2011

**TPC Vice-Chair**, *IEEE Device Research Conference (DRC)*, University of California, Santa Barbara, CA, June 2011

**Chair**, *Quantum, Power, and Compound Semiconductor Devices Sub-Committee, IEEE International Electron Devices Meeting (IEDM '10)*, San Francisco, California, December 2010

**Organizer and Chair**, *Rump Session on Embedded Memory called “Looking for Extra Cache”, IEEE Device Research Conference (DRC '10)*, Univ. of Notre Dame, June 2010

*Last updated, Dec 2015*

**Organizer and Chair**, *Rump Session on Steep Slope Transistors called “Steep Slope or Slippery Slope”*, *IEEE Device Research Conference (DRC '10)*, Penn State University, June 2009

**TPC Member**, *IEEE Device Research Conference (DRC '10)*, Univ. of Notre Dame, June 2010

**TPC Member**, *Electronic Materials Conference (EMC '10)*, Univ. of Notre Dame, June 2010

**TPC Member**, *Semiconductor Interface Specialist Conference (SISC '10)*, San Diego, California, December 2010

**TPC Member**, *European Solid-State Device Research Conference (ESSDERC '09)*, Seville, Spain, September, 2010

**TPC Member**, *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED '10)*, Austin, Texas, August 2009

**TPC Member**, *European Solid-State Device Research Conference (ESSDERC '09)*, Athens, Greece, September, 2009

**TPC Member**, *Quantum, Power, and Compound Semiconductor Devices, IEEE International Electron Devices Meeting (IEDM '09)*, Baltimore, Maryland, December 7–9, 2009

**TPC Member**, *IEEE Device Research Conference (DRC '09)*, Penn State Univ., June 2009

**TPC Member**, *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED '09)*, San Francisco, California, August 2009

**TPC Member**, *European Solid-State Device Research Conference (ESSDERC '09)*, Edinburgh, Scotland, September 2008

**TPC Member**, *Silicon Nanoelectronics Workshop (SNW '08)*, Honolulu, Hawaii, June 2008

**TPC Member**, *International Symposium on VLSI Technology, Systems, and Applications (2005 IEEE VLSI-TSA)*, Hinshu, Taiwan, April 25-27, 2005

**Arrangements Chair**, *IEEE Device Research Conference (DRC)*, Penn State University, June 2009

**Panel Chair**, *ACM/IEEE International Symposium Low Power Electronics and Design (ISLPED '09)*, San Francisco, California, August 2009

**Session Chair**, *“Non Volatile Memory” at the High-K Dielectric Materials and Gate Stack Symposium, Electrochemical Society Meeting (ECS '09)*, Vienna, Austria, October 2009

**Session Chair**, *“MOS Devices” at the IEEE Device Research Conference (DRC '09)*, June 2009

**Session Chair**, “*MOS Devices*” at the *IEEE Device Research Conference (DRC ‘09)*, June 2009

**Session Co-Chair**, “*III-V Logic Transistors with Advanced Gate Stack*” at the *IEEE International Electron Devices Meeting (IEDM ‘09)*, Baltimore, Maryland, December 8, 2009

**Session Co-Chair**, “*Heterostructure High-Speed Devices*” at the *IEEE International Electron Devices Meeting (IEDM ‘08)*, San Francisco, California, December 2008

**Session Chair**, “*Materials for Ge and Si devices*” at the *International Conference on Insulating Films on Semiconductors (INFOS ‘07)*, Athens, Greece, June 2007

**NSF Review Panelist**- In EPDT, EMT programs in years 2008-2010

**Reviewer,**

NanoLetters

Nature Materials

Nature Communications

IEEE Transactions on Nanotechnology

IEEE Transactions on Electron Devices

IEEE Electron Device Letters

ACM Journal on Emerging Technologies in Computing Systems

Solid-State Electronics

Applied Physics Letters

Journal of Applied Physics

Journal of Vacuum Science and Technology B

Journal of Nanotechnology

Nanotechnology (Journal) from Institute of Physics (IOP)

Journal of Electronic Materials

IEDM, DRC, ESSDERC, VLSI-TSA, IEEE ISLPED, SISC, EMC, IEEE SNW