Siddharth Joshi

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Academic Positions

Assistant Professor — **University of Notre Dame**
Aug 2018 - current — Department of Computer Science and Engineering

Postdoctoral Scholar — **University of California, San Diego**
July 2017 - July 2018 — Deptartment of Bioengineering
Supervisor: Gert Cauwenberghs
Resource Constrained Machine Intelligence: Analog and mixed-signal, MIMO, signal processing and brain inspired computing for extremely efficient computing.

Education

Ph.D. — **University of California, San Diego**
2011-2017 — Department of Electrical and Computer Engineering
Advisor: Gert Cauwenberghs
Thesis Title: *"High-Fidelity Spatial Signal Processing in Low-Power Mixed-Signal VLSI Arrays".*

M.S. — **University of California, San Diego**
2009-2011 — Electrical and Computer Engineering
Specialization: Computer Engineering

B.Tech. — **Dhirubhai Ambani Institute of Information and Communication Technology**
2004-2008 — Information and Communication Technology

Relevant Publications

- **S Joshi**, C Kim, CM Thomas, G Cauwenberghs, "Digitally Adaptive High-Fidelity Analog Signal Processing Insensitive to Capacitive Multiplying DAC Inter-Stage Gain Error," to appear *IEEE Transactions on Circuits and Systems I.*
- S Kalyan **S Joshi**, S Sheikh, BU Pedroni, G Cauwenberghs, "Unsupervised Synaptic Pruning Strategies for Restricted Boltzmann Machines," to appear, *BioCAS*, 2018
- **S Joshi**, BU Pedroni, G Cauwenberghs, "Neuromorphic Event-Driven Multi-Scale Synaptic Connectivity and Plasticity" *51st Asilomar Conference on Signals, Systems and Computers*, Oct. 31, 2017
- F Broccard, **S Joshi**, J Wang, G Cauwenberghs, "Neuromorphic neural interfaces: from neurophysiological inspiration to biohybrid coupling with nervous systems," *Journal of Neural Engineering*, 14.4 (2017): 041002.
- SB Eryilmaz, E Neftci, **S Joshi**, S Kim, M BrightSky, HL Lung, C Lam, G Cauwenberghs, HSP Wong, "Training a Probabilistic Graphical Model With Resistive Switching Electronic Synapses," *IEEE Transactions on Electron Devices*, vol. 63 (12) pp 5004-5011 2016.
- J Park, T Yu, **S Joshi**, C Maier, G Cauwenberghs, "Hierarchical Address Event Routing for Reconfigurable Large-Scale Neuromorphic Systems," *IEEE Transactions on Neural Networks and Learning Systems*, vol 1-15, no 99, 2016.
- EO Neftci, BU Pedroni, **S Joshi**, M Al-Shedivat, G Cauwenberghs, "Stochastic Synapses Enable Efficient Brain-Inspired Learning Machines," *Frontiers in Neuroscience* vol. 10, pp. 241:1-16, 2016.
- **S Joshi**, C Kim, S Ha, G Cauwenberghs, "From Algorithms to Devices: Enabling Machine Learning through Ultra-Low-Power VLSI Mixed-Signal Array Processing," *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Apr. 2017

- S Hamdioui, S Kvatinsky, G Cauwenberghs, L Xie, N Wald, **S Joshi**, HM Elsayed, H Corporaal, K Bertels, "Memristor for computing: Myth or reality?," *Design, Automation & Test in Europe Conference & Exhibition (DATE)* 2017 Mar 27 (pp. 722-731). IEEE.
- **S Joshi**, C Kim, S Ha, YM Chi, G Cauwenberghs, "2pJ/MAC 14b 8×8 Linear Transform Mixed-Signal Spatial Filter in 65nm CMOS with 84dB Interference Suppression," *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, 2017, pp. 364-365.
- BU Pedroni, S Sheik, **S Joshi**, G Detorakis, S Paul, C Augustine, EO Neftci, G Cauwenberghs, "Forward table-based presynaptic event-triggered spike-timing-dependent plasticity," *Proc. IEEE Biomedical Circuits and Systems (BioCAS)*, Shanghai, China, Oct. 17-19, 2016.
- SB Eryilmaz, **S Joshi**, EO Neftci, W Wan, G Cauwenberghs, HSP Wong, "Neuromorphic architectures with electronic synapses," *2016 17th International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, CA, 2016.
- T Yu, J Park, **S Joshi**, C Maier, G Cauwenberghs, "65k-neuron integrate-and-fire array transceiver with address-event reconfigurable synaptic routing," *Proc. IEEE Biomedical Circuits and Systems Conf. (BioCAS)*, Hsinchu Taiwan, Nov. 28-30, 2012.
- T Yu, J Park, **S Joshi**, C Maier, G Cauwenberghs, "Event-driven neural integration and synchronicity in analog VLSI," *Proc. IEEE Engineering in Medicine and Biology Conf. (EMBC)*, San Diego CA, Aug. 28-Sept. 1, pp. 775-778, 2012.
- J Park, T Yu, C Maier, **S Joshi**, G Cauwenberghs, "Live Demonstration: Hierarchical Address-Event Routing Architecture for Reconfigurable Large Scale Neuromorphic Systems,", *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, Seoul Korea, May 20-23, pp. 707-711, 2012.
- T Yu, **S Joshi**, V Rangan, and G Cauwenberghs, "Subthreshold MOS Dynamic Translinear Neural and Synaptic Conductance," *Int. IEEE/EMBS Conf. Neural Engineering (NER)*, Cancun, Mexico, Apr. 27-May 1, pp. 68-71, 2011.
- **S Joshi**, S Deiss, M Arnold, J Park, T Yu, G Cauwenberghs,"Scalable Event Routing in Hierarchical Neural Array Architecture with Gobal Synaptic Connectivity, " *Proc. IEEE Int. Workshop Cellular Nanoscale Networks and Their Applications (CNNA)*, Berkeley CA, Febr. 3-5, 2010.
- BY Kumar, **S Joshi**, S Patkar, H Narayanan, "FPGA based High Performance Double-precision Matrix Multiplication," *Proc. 22nd Int. Conference on VLSI Design.* New Delhi, India, 2009.

Invited Talks

- "Scalable, Event-Driven, Multi-Scale Synaptic Connectivity and Plasticity in Neuromorphic Systems" **S Joshi**, UC, San Diego, Institute for Neural Computation, Dec., 2017.
- "Neuromorphic Event-Driven Multi-Scale Synaptic Connectivity and Plasticity" **S Joshi**, *51st Asilomar Conference on Signals, Systems and Computers*, Oct. 31, 2017.
- "High-Fidelity Spatial Signal Processing in Low-Power Mixed-Signal VLSI Arrays" **S Joshi**, IIT-Kharagpur, India, Jun. 23, 2017.
- "From Algorithms to Devices: Enabling Machine Learning through Ultra-Low-Power VLSI Mixed-Signal Array Processing," **S Joshi**, C Kim, S Ha, G. Cauwenberghs, *IEEE Custom Integrated Circuits Confrence (CICC)*, Austin, Tx, Apr. 3, 2017.
- "Memristor For Neuromorphic Computing," **S Joshi**, H Mustafa, G. Cauwenberghs, *2017 Design, Automation & Test in Europe (DATE)*, Swisstech, Lausanne, Switzerland, Mar. 27 – 31, 2017.
- "Integrated Circuits for Extremely Energy Efficient Collective Electronics", *NSF-SRC, Energy-Efficient Computing: from Devices to Architectures (E2CDA) kick-off meeting*, Gaithersburg, MD, Oct. 18, 2016.
- "Spectral and Spatial Analog Signal Processing for MIMO Transceivers," **S Joshi**, C Kim, G Cauwenberghs, IIT-Kharagpur India, Jun. 6, 2016.
- "Mapping Vision Algorithms on a Neuromorphic Array Architecture," **S Joshi**, SB Eryilmaz, G Cauwenberghs , HSP Wong, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose CA, Nov. 3, 2014.